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TECHNIQUES FOR ON-WAFER RELIABILITY TESTING FOR MMICs

TRW Space & Electronics Group

Yoshio Saito

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13. ABSTRACT (Maximum 200 words)

Two Compliant Interconnected Structures (CISs) have been designed and fabricated to enable accelerated DC life tests to be performed at the wafer level. The first CIS was fabricated using Kapton polyimide, the second with borosilicate glass. Both structures are capable of providing bias to the GaAs wafers at 240°C for an extended period of time. Three inch wafers that contain process test characterization vehicles, a distribution amplifier, and three-stage amplifiers, were used to demonstrate the feasibility of the techniques.

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TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

1. EXECUTIVE SUMMARY

1.1 INTRODUCTION

In the last several years, significant progress was made in development of state-of-the-art performance of GaAs MMIC in MMIC Phases 1 and 2. In addition, manufacturability of GaAs MMIC was also demonstrated. Because of this excellent progress, insertion of GaAs MMICs into a variety of DoD and NASA electronic systems such as radars, communications, electronic counter measures, and smart munitions is in progress. However, reliability of GaAs devices/MMICs still remain to be an issue, and TRW is determined to ensure mission requirements are met. In addition, sufficient quantities and reasonable manufacturing cost are also essential. In order to meet these, wafer level reliability testing technique is essential. A "good die" concept should be implemented for cost reduction of GaAs MMIC manufacturing.

TRW has undertaken an innovative approach to this program to meet the requirements of "on-wafer reliability testing of GaAs MMICs." The approach is to insert the compliant interconnect (COIN) technology to on-wafer reliability testing. We named this program, compliant interconnect structure (CIS). The uniqueness of this approach is to perform accelerated dc life test on wafer level using the CIS with a life test fixture in the high-temperature oven.

1.2 PROGRAM GOALS

- Develop a reliability testing method for MMICs at wafer level.
- Perform life tests using the developed on-wafer reliability testing methodology and correlate the reliability data between on-wafer and packaged MMICs.

1.3 SUMMARY

TRW has proved the concept of on wafer level reliability testing at elevated temperature. We designed and manufactured two types of standard evaluation circuit (SEC), and six types of technology evaluation vehicle (TCV) for on-wafer reliability testing. We successfully designed and fabricated the CIS for this program and proved that the electrical contact was made between SECs and TCVs on GaAs wafer, and dc bias on ceramic plates. With TRW's capfab funding, the life test fixture for on-wafer reliability testing was

designed and fabricated. We focused on developing a functional CIS, therefore there was no time or funds available to perform accelerated life testing.

2. ON-WAFER RELIABILITY STUDY

2.1 MMIC DESIGN AND FABRICATION

We selected the 0.5 μm MESFET technology for this program because it is the most mature process and is supported by the following reliability test data.

2.1.1 Mask Layout

Figure 1 shows mask layout for on-wafer reliability testing. There are a total of 52 reticles on a three-inch wafer. For on-wafer and packaged SEC life test, we laid out a half wafer rotated at 180 degrees so that on-wafer life test can be performed on both sides of the wafer with one-design of CIS. A total of six alignment marks were put on for wafer-to-CIS alignment.

2.1.2 PM, TCVs, and SECs

We have had a standardized PM pattern for 0.5 μm MESFET technology since 1985 that is being used in high-reliability wafer production. Thus, we incorporated this PM pattern into Mask design for on-wafer reliability testing (OWR). Figure 2 defines the test elements that comprise the 0.5μm MESFET PM, and it describes the key process parameter for each PM pattern. This PM captures all the key MESFET process steps; PM patterns are used for in-process MMIC characterization. Figure 3 defines the TCV and SEC elements and test parameters for the baseline 0.5μm MESFET technology. These patterns serve multiple functions. The field-effect transistor

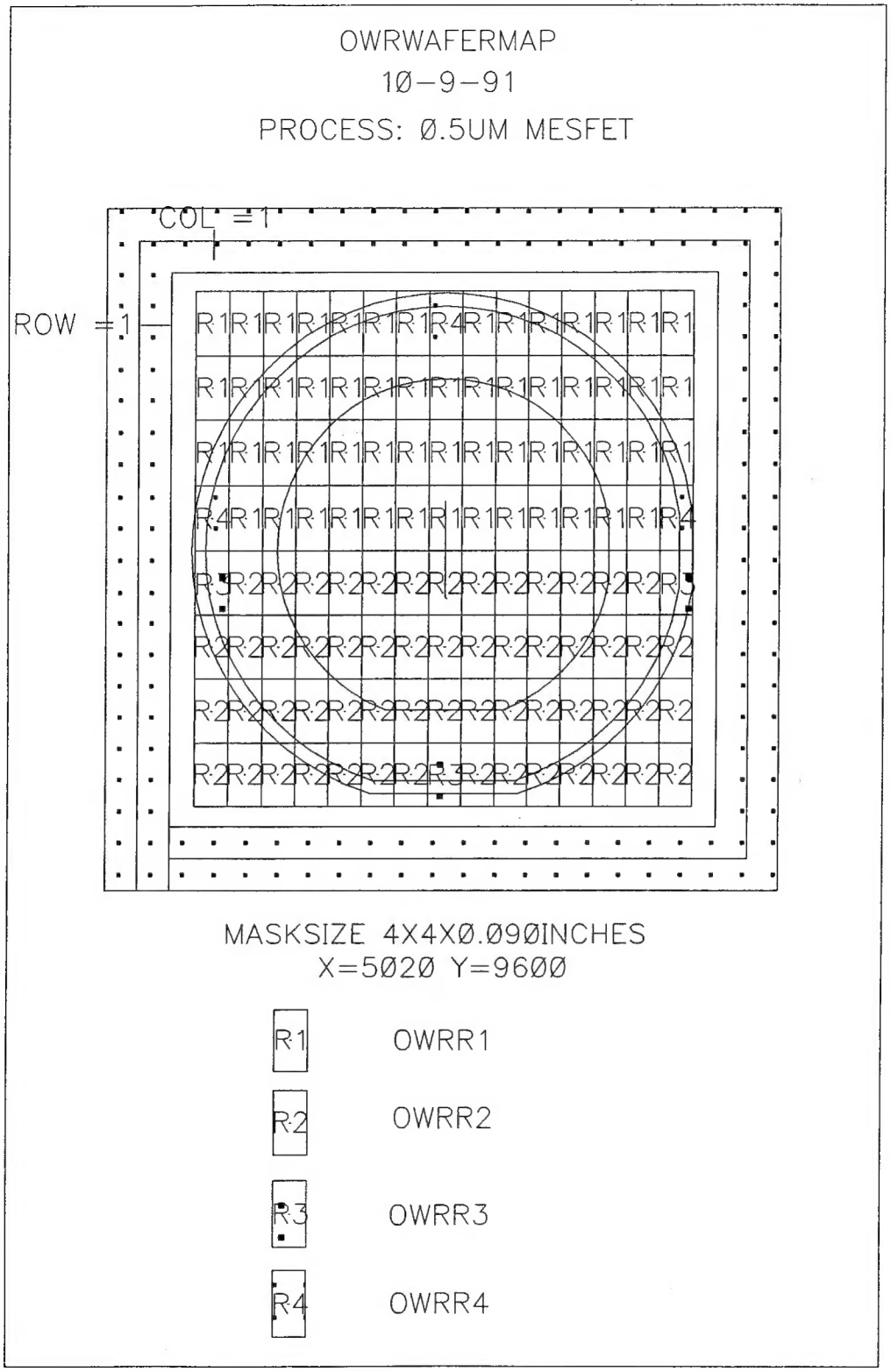


Figure 1. Mask Layout

DEVICE	PARAMETER	MIN	MAX	UNITS	CORRELATION
ABSTR	Ab_11	–	10	Ohm	Rc OF FIC TO SIC
	Ab_21	–	10	Ohm	
RSNP	Rsnp	100	200	Ohm/sq	Rsh OF n+ CHANNEL
RCTFR	Rctfr	0.0001	100	Ohm	Rc OF FIC TO TFR
RSGAT	Rsgate	0.05	0.10	Ohm/sq	Rsh OF GATE METAL
RSNM	Rsnm	100	200	Ohm/sq	Rsh OF n- CHANNEL
RSNPNM	Rsnpnm	100	200	Ohm/sq	RSH OF n- and n+ IMPLANTS
RCOC	Rcoc	–	10	Ohm	Rc OF OHMIC METAL TO GaAs
RSOC	Rsoc	0.0001	0.1	Ohm/sq	Rsh OF OHMIC CONTACT REGION
RSTFR	Rstfr	80	120	Ohm/sq	Rsh OF TFR
RSFIC	Rsfic	0.02	0.07	Ohm/sq	Rsh OF FIC
RSSIC	Rssic	0.005	0.015	Ohm/sq	Rsh OF SIC
MIMCAP	BVCap08	10	40	Volts	BV OF 8pF CAPACITOR
	Cap08	5	10	pF	MEASURED CAPACITOR VALUE OF Cap08
GSIZE	Gsize	0.01	1.0	µm	GATE LENGTH
TFRSIZE	Tfrsize	5	15	µm	WIDTH OF TFR STRIP
FICSIZE	Ficsize	5	15	µm	WIDTH OF FIC STRIP
OCSIZE	Ocsize	5	15	µm	WIDTH OF OHMIC CONTACT STRIP

Figure 2. Elements and Test Specifications

(FET)/isolation (ISO) in-process FET is used as a guide during gate formation to properly target the recess depth. The dc/RF FET pattern (LNI300P) qualifies dc/RF performance of the active devices contained on the MMIC circuits.

TCVs are designed to characterize specific reliability parameters such as electromigration of FIC, gate metal, air bridge, etc., and ohmic metal degradation. Figures 4 through 8 describe all TCVs designed for this program. As shown in Figures 3, the contact pads were made to be 150x150 μm for easier contact with CIS.

We incorporated two types of SEC in the reticle; one is a distributed amplifier (DA) designed to operate at 1-5 GHz, and the other is a three-stage amplifier (XBC1) designed to operate at 8-15 GHz. However, because all drain pads of the three-stage amplifier were connected, the circuit exhibited a severe oscillation. Therefore, we can only use DAs for the dc life test. The DA does not oscillate because it is a low gain single stage amplifier. In one reticle, there are two XBC1s (one has enlarged pads with three drain lines connected, and another one is a normal

A. TCV TESTING

DEVICE	PARAMETER	MIN	MAX	UNITS	CORRELATION
FATFET	I_{dss}	0.1	5.0	mA	Ids AT Vds-3V, Vg=0V
	Idmin			mA	[]
	Vpo	-3.5	-1.5	V	PINCH-OFF VOLTAGE
	Npeak	3.0E17	3.5E17	cm-3	PEAK CONCENTRATION
	Dpeak	0	1.0	µm	DEPTH OF Npeak
	Dtail	1.0	2.0	µm	DEPTH OF tail
FET/ISO	I_{dss}	17.5	32.5	mA	TOTAL CURRENT
	Gm50	15	25	mS	TRANSCONDUCTANCE AT Ids=50% I_{dss}
	VP02	-3.0	-1.0	V	PINCH-OFF VOLTAGE AT Ids=2% I_{dss}
	BVgsx	-10.0	-1.0	V	Vgs at Vds=3V, Vs=0V
	BVisol	5	40	V	VOLTAGE ACROSS 1 µm GAP AT Iisol=20.0uA
RCOC CHAIN	Rcoc_ch	50	300	Ohm	RESISTANCE OF OHMIC METAL TO n+, 30 CONTACTS
RCTFR CHAIN	Rctfr_ch	100	300	Ohm	RESISTANCE OF FIC TO TFR, 30 CONTACTS
FIC-FIC-FIC	Fic1thru	1	15	Ohm	FIC ELECTROMIGRATION
	Fic2thru	1	15	Ohm	
	Fic3thru	1	15	Ohm	
	Fic21iso	1	200	Mohm	
	Fic23iso	1	200	Mohm	
FIC-TFR-FIC	Fic1thru	1	20	Ohm	TFR ELECTROMIGRATION
	Tfrthru	2	25	KOhm	
	Fic2thru	1	20	Ohm	
	Tfrfic1iso	1	200	MOhm	
	Tfrfic2iso	1	200	MOhm	
VIA CHAIN	Rviachout	0.1	5	Ohm	NITRIDE INTEGRITY, FIC TO TOP METAL RESISTANCE
	Rviachin	1	10	Ohm	
TM-TM-TM	Tm1thru	0.1	5	Ohm	TOP METAL ELECTROMIGRATION
	Tm2thru	1	10	Ohm	
	Tm3thru	1	10	Ohm	
	Tm21iso	1	100	Mohm	
	Tm23iso	1	100	Mohm	

B. TCV TESTING - LN1300P - 300 µFET

TEST	PARAMETER	MIN	MAX	UNITS	CORRELATION
DC	I_{dss}	51	87	mA	Ids at Vds =3V, Vg=0V
	Gm50	33	-	mS	TRANSCONDUCTANCE AT 50% PINCH-OFF POINT
	Vp02	-2.8	-1.5	V	Vg AT Ids=2% I_{dss}
	BVgsx	6	-	V	Vg AT Vs=0V, Vd=3.0V, Ig=0.3mA
RF	S-parameters	-	-	-	S-PARAMETERS COLLECTED FOR DEVICE MODELING
	MAG18	6	-	-	MAXIMUM AVAILABLE GAIN AT 18 GHz
	Ft	16	-		UNITY GAIN BANDWIDTH
	IP_3	23	-	dBm	THIRD ORDER INTERCEPT POINT
DELTA LIMITS	DELTA I_{dss}	-	25	PERCENT	TOTAL CURRENT
	DELTA Gm50	-	10	PERCENT	TRANSCONDUCTANCE
	DELTA BVgsx	-	20	PERCENT	GATE-TO-SOURCE BREAKDOWN VOLTAGE

C. SEC TESTING - DISTRIBUTED AMPLIFIER

TEST	PARAMETER	LOW LIMIT	HIGH LIMIT	UNITS	CORRELATION
ON STATE	Ids	-	98	mA	TOTAL CURRENT (DC)
	G	1	7	dB	GAIN
	RL (IN)	11	-	dB	INPUT RETURN LOSS
	RL (OUT)	11	-	dB	OUTPUT RETURN LOSS
	IP_3	20	-	dBm	THIRD ORDER INTERCEPT POINT
OFF STATE	ISOL	20	-	dB	ISOLATION
DELTA LIMITS	DELTA Ids	-	20	PERCENT	TOTAL CURRENT
	DELTA G	-	0.5	dB	GAIN
	DELTA ISOL	-	4	dB	ISOLATION
	DELTA IP_3	-	4	dBm	THIRD ORDER INTERCEPT POINT

16384 3950_1028

Figure 3. TCV and SEC Elements and Test Specifications

TM_TCV
Top metal TCV with periodic airbridge

Description:
This structure is used to stress top metal line. It is a 7.0 μm wide and 3.32 mm long serpentine line on gallium arsenide substrate. The spacingbetween neigboring linea is 7.0 μm.

Test condition:
1) Measure V_{85} @ I_{14} = 56 mA,
$R_{top\ metal} = V_{85}/I_{14}$

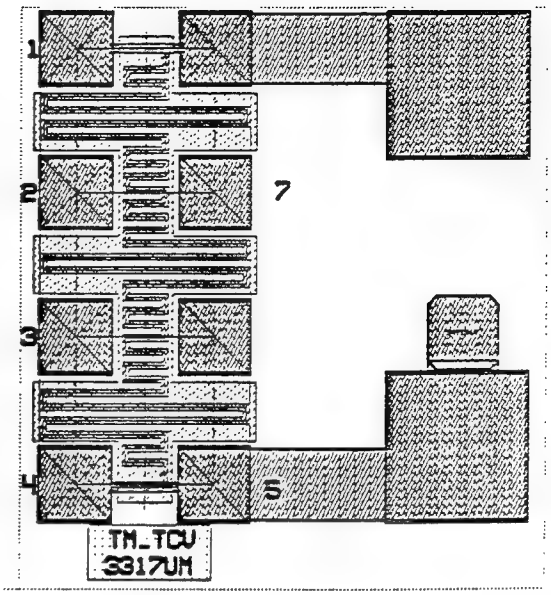


Figure 4. Layout of Top Metal TCV

TFR-TCV:
Thin film resistor TCV

Description:
This structure is used to stress thin film resistor with maximum current density. It has two TFR resistors. One is 10 μm x 300 mm (3.3KΩ) and the other is 50 μm x 30 μm (67Ω).

Test condition:
1) Measure V_{13} @ I_{86} = 3.0 mA,
$R_{oc} = V_{86}/I_{13}$
2) Measure V_{34} @ I_{65} = 15 mA,
$R_{oc} = V_{65}/I_{34}$

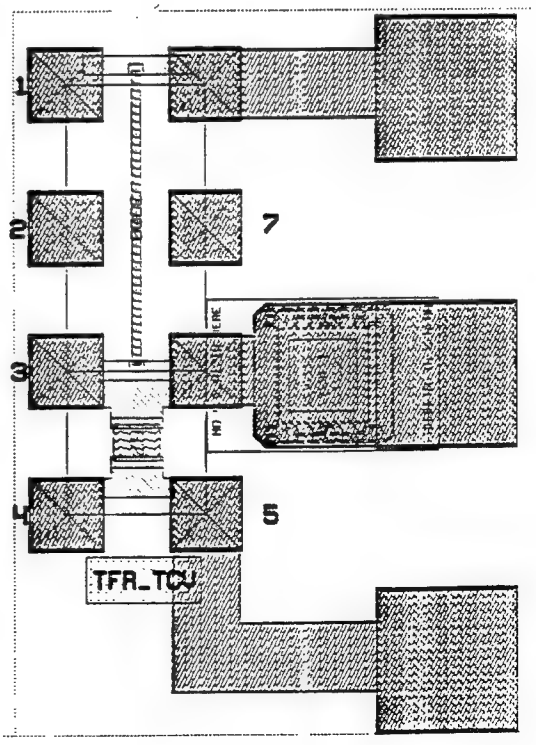


Figure 5. Thin Film Resistor TCV

Technology Characterization Vehicle:

OC-TCV:
Ohmic Contact TCV

Description:
This structure is used to stress the ohmic contact and measure the degradation. There are 12 48 μm x 16 μm contacts. the current path includes: 1) FIC to ohmic metal contact, 2) Ohmic contact to active layer, and 3) Active layer

Test condition:
1) Measure V_{85} @ I_{14} = 24 mA,
$R_{oc} = V_{85}/I_{14}$

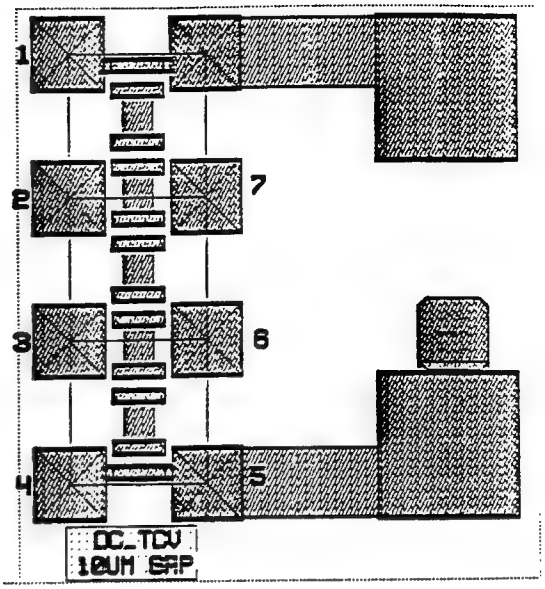


Figure 6. Ohmic Contact TCV

GATE_TCV
Gate metal TCV

Description:
This structure is used to stress gate metal line. It is a 0.5 μm wide and 3.32 mm long serpentine line. The spacingbetween neigboring linea is 13.5 μm.

Test condition:
1) Measure V_{85} @ I_{14} = 1.0 mA,
$R_{gate} = V_{85}/I_{14}$

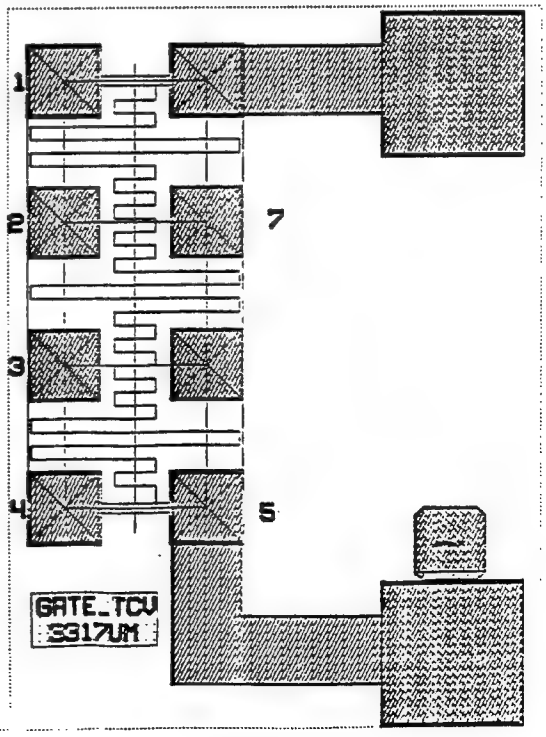


Figure 7. Gate Metal TCV

AB_TCV
Top metal TCV with periodic airbridge

Description:
This structure is used to stress top metal line. It is a 7.0 µm wide and 3.53 mm long serpentine line with periodic airbridge. The touch down on gallium substrate is 70 µm x 7.0 µm. The spacingbetween neigboring linea is 7.0 µm.

Test condition:
1) Measure V_{85} @ I_{14} = 56 mA,
$R_{top\ metal\text{-}AB} = V_{85}/I_{14}$

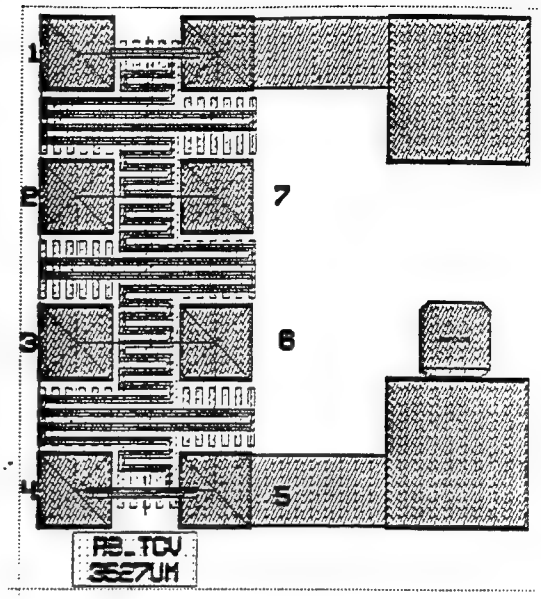


Figure 8. Top Metal TCV

XBC1) and four DAs (one has enlarged contact pads, and the other three are normal DAs packaged for SEC life test). The drain lines are connected for reducing a number of contact pads; one contact bumps instead of three. In the packaged XBC1 lifetest, all three drain pads are wirebonded to the same bias pin.

A schematic diagram and layout of the DA and XBC1 are shown in Figures 9, 10 and 11, 12, respectively. This circuit contains all passive and active elements which are representative of MESFET MMIC technology.

The elements on the DA are:

- FETs (225μm wide) - 3 each
- Plated micro strip line (various width) - 19 sections
- Ground vias - 6 each
- Air bridges - 6 each FET and capacitor
- Capacitors - 2 each
- Thin film resistors - 2 each
- 5 mil bonding/RF probe pads - 6 each
- 5 mil internal dc probe pads - 2 each.

The elements on the XBC1 are:

- MESFETs (300 μm wide) - 3 each
- MESFETs (150 μm wide) - 2 each
- MESFET (75 μm wide) - 1 each
- Plated Microstrip lines - many
- Ground Vias - 11 each
- Abridges - 21 each
- Capacitors - 15 each
- Thin Film Resistors - 6 each
- Inductors - each.

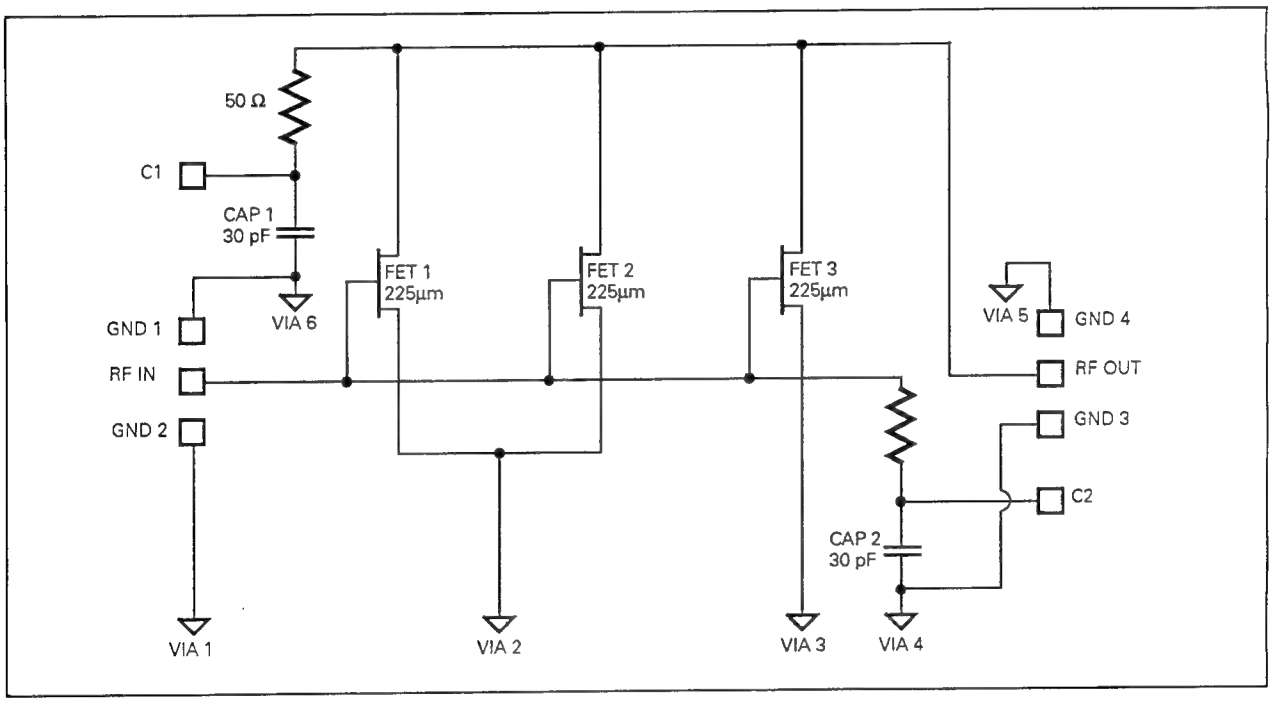


Figure 9. SEC Distributed Amplifier Schematic

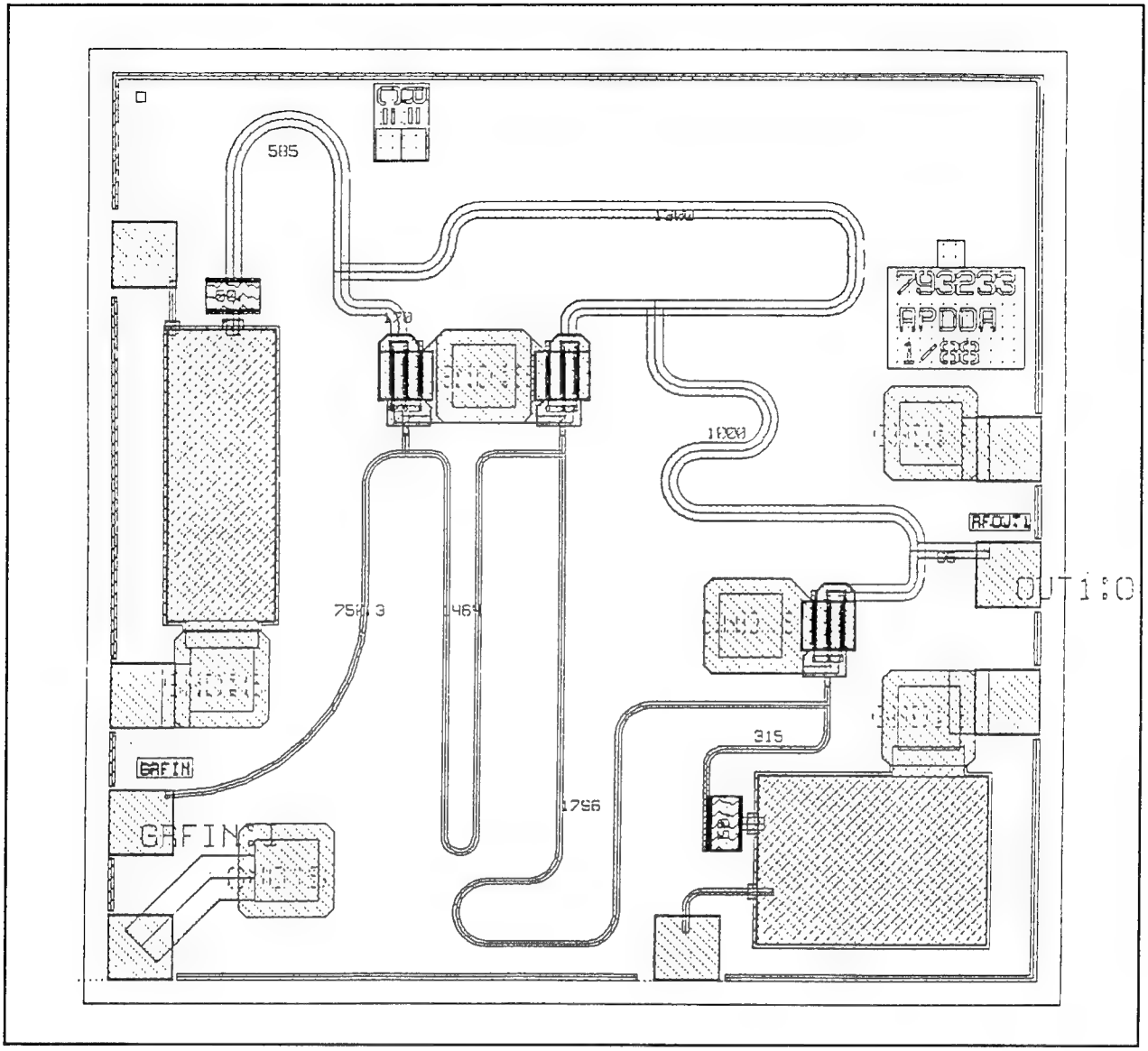


Figure 10. SEC Schematic Diagram

Three Stage X-Band Amplifier
(Chip #1)

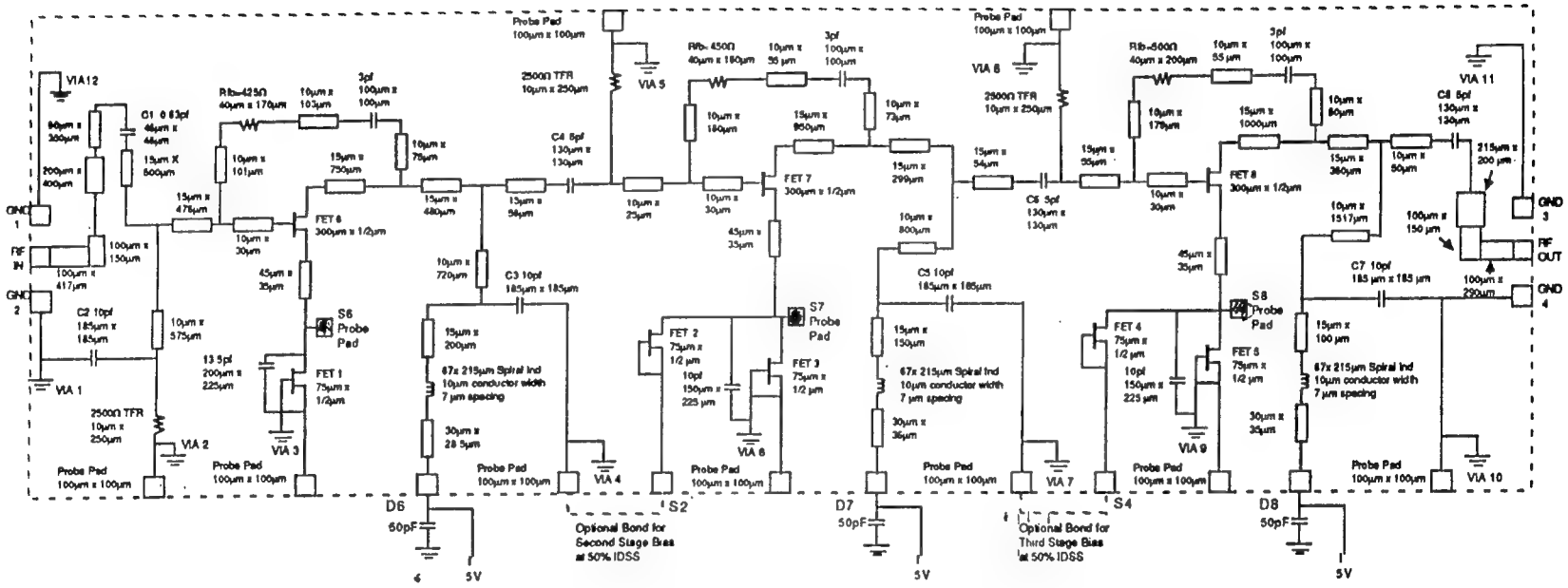


Figure 11. XBC1 Circuit Schematic Diagram

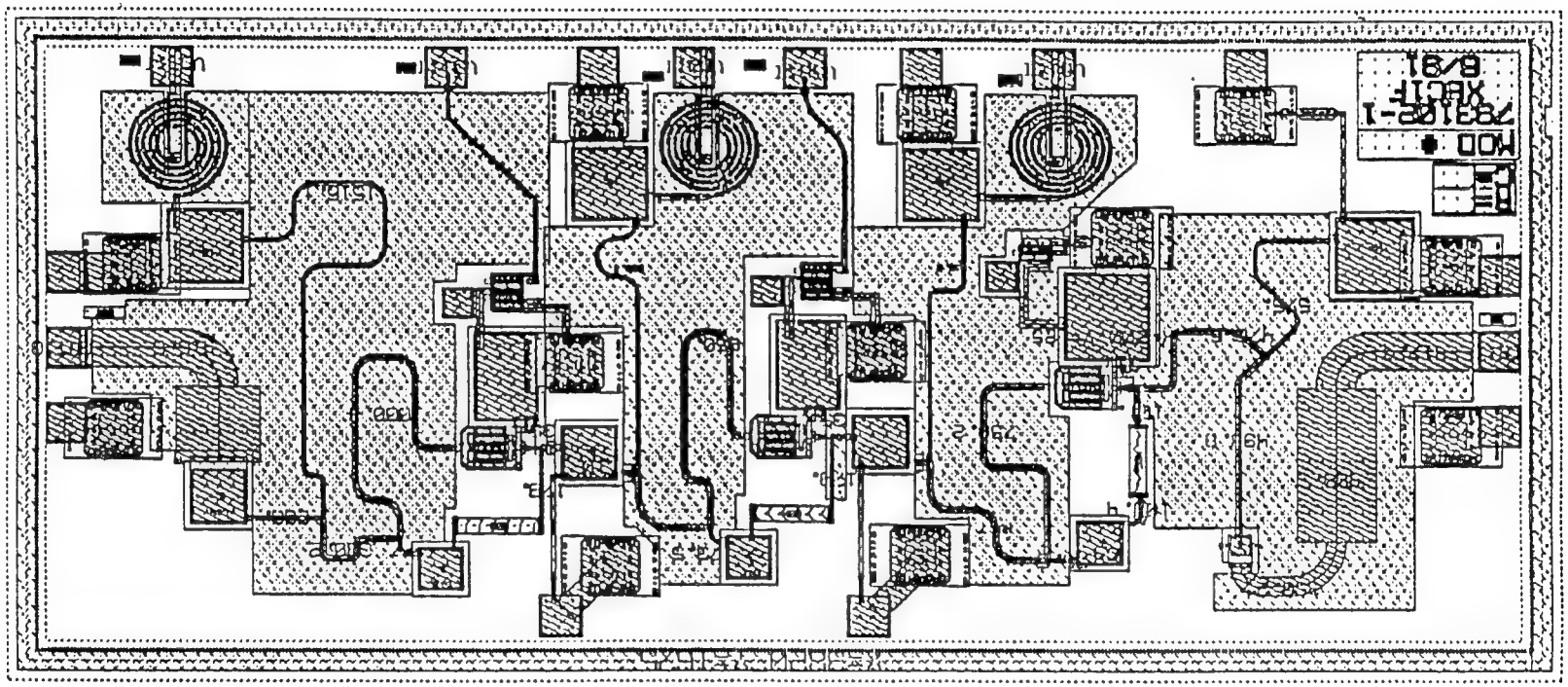


Figure 12. XBC1 Layout

2.1.3 Wafer Fabrication

Wafers were fabricated in TRW's new wafer manufacturing line (D1) with a well established base line process. We have qualified GaAs production line in Building R6 and manufactured 0.5μm MESFET MMICs and delivered approximately 3000 chips to classified programs in 1988-1992. In mid 1993, we qualified GaAs manufacturing line in Building D1. Wafer fabrication for this program was completed in approximately the same time frame as D1 line qualification of 0.5 μm MESFET.

Figure 13 illustrate wafer fabrication flow diagram. Epitaxy materials were grown by MBE on a three-inch wafer with standard MESFET profile. Active devices were isolated by both mesa etch and ion implantation. Conventional 0.5 μm gate was written by electron beam lithography (EBL).

2.1.4 In-Process PM Characterization

We have implemented a trend chart in both critical and non critical nodes during the wafer processes. Appendix-A shows PCM data at a critical node for "On-wafer reliability lot 4 (OWR-4)."

The most critical node for MMIC reliability is at top metal testing: PCMs were tested for pre and post thermal stabake at 240°C for 48 hours. The most important parameter at stabake is Idss deltas. We set a delta limit of Δ6%. Both OWR-1 and 2 had higher delta Idss and the OWR-2 stabake result is shown in Figure 14. One half of the wafer exhibited much higher Idss deltas. We believe the cause of this high Idss delta was due to contamination of gate metals, not the fat gate.

However, we were unable to explain why one half wafer had consistently higher Idss deltas. In the past, we have experienced high delta Idss (~10-20%) due to the fat gate (Au spilling over Ti/Pt metal and causing Au diffusion into

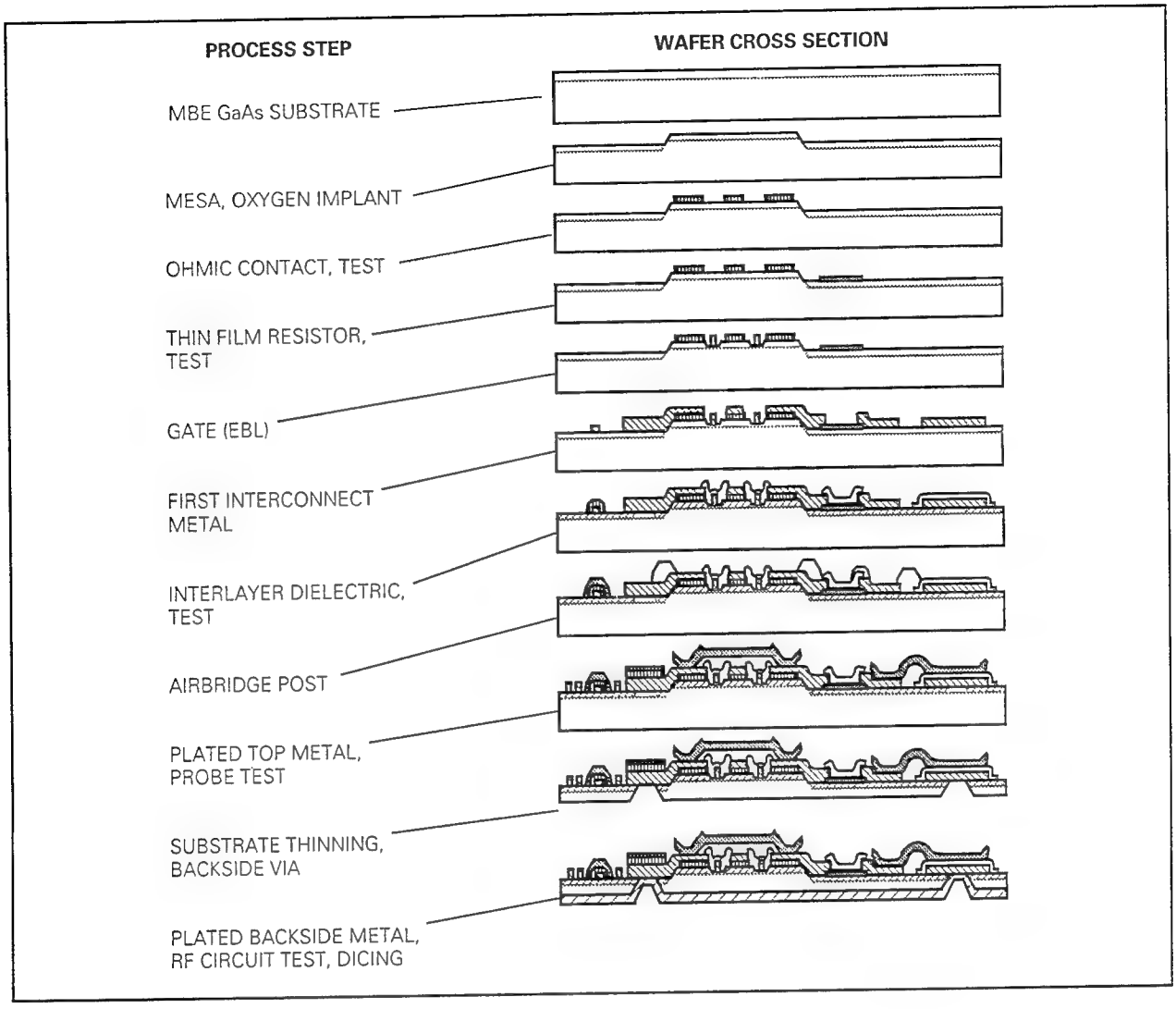


Figure 13. 0.5 μm MESFET Baseline Process Flow

GaAs). However, in OWR-1 and 2 case we did not observe fat gate. The OWR-4 lot resulted in excellent stabake deltas as shown in Figure 15.

Figures 16 through 21 show the trend charts of 0.5μm MESFET in process testing of PCM. Most of the parameters are within three sigma of average values. When the parameters are over the three sigma limit for seven consecutive wafers, the process is halted until the problem is resolved. A responsible engineer(s) will be assigned to investigate the anomaly. When the problem(s) are solved, In process Corrective Action Board (ICAB) will close out the

PRE/POST STABAKE TEST AT COMPLETION OF TOP METAL

STABAKE AT 240°C FOR 48 HOURS

LOT NO: ORW-2

WAFER NO: 177-138

Idss (mA)

		C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14
R2	PRE BAKE			54	56.2	60.3	63.9	59.9	59.4	58.3	57.1			
	POST BAKE			43.3	44	48	52.6	48	47.7	44.2	48.7			
	DELTA (%)			-19.81	-21.71	-20.40	-17.68	-19.87	-19.70	-24.19	-14.71			
R3	PRE BAKE	53.2	55.4	57.4	57.6	60.5	63.5	63.3	60.3	61.7	59.6	55.1	51.6	38.3
	POST BAKE	41.7	40.3	41.6	44.4	47.6	51.1	48.7	42.6	44.7	43.7	40.7	36.7	24.3
	DELTA (%)	-21.62	-27.26	-27.53	-22.92	-21.32	-19.53	-23.06	-29.35	-27.55	-26.68	-26.13	-28.88	-36.55
R4	PRE BAKE	52.2	50.8	55.5	58.5	64.6	65	61.4	64.2	60.7	58.6	55.7	53.8	51.3
	POST BAKE	44.2	37.2	39.4	42.2	47	48.1	45.2	47	43	40.7	39.9	36.7	34.6
	DELTA (%)	-15.33	-26.77	-29.01	-27.86	-27.24	-26.00	-26.38	-26.79	-29.16	-30.55	-28.37	-31.78	-32.55
R5	PRE BAKE	50.2	49.3	53.2	56.5	57.4	58.7	61.2	59.5	57.4	56.4	54.8	51.5	48.5
	POST BAKE	29.5	28.9	33.7	37.6	38.7	40	42.9	40.7	38.1	37.3	35.6	32.2	27.7
	DELTA (%)		-41.38	-36.65	-33.45	-32.58	-31.86	-29.90	-31.60	-33.62	-33.87	-35.04	-37.48	-42.89
R6	PRE BAKE		50.1	53.3	58.1	58.9	59.5	60.1	58.7	58.3	57.7	56.4	53.7	
	POST BAKE		26.4	33.4	38.9	39	40.1	40.8	39.1	38.9	37.5	36.7	32.9	
	DELTA (%)		-47.31	-37.34	-33.05	-33.79	-32.61	-32.11	-33.39	-33.28	-35.01	-34.93	-38.73	
R7	PRE BAKE			54.9	55.4	55.6	57.4	56.7	57.7	57.4	56.2			
	POST BAKE			34.3	34.5	34.6	36.7	36.8	37.6	36.6	37.2			
	DELTA (%)			-37.52	-37.73	-37.77	-36.06	-35.10	-34.84	-36.24	-33.81			
	AVE DELTA	-31.30												

Figure 14. Summary of Stabake Deltas of OWR-2 Lot

PRE/POST STABAKE TEST AT COMPLETION OF TOP METAL

STABAKE AT 240°C FOR 48 HOURS

LOT NO: ORW-4
WAFER NO: 206-063
Idss (mA)

		C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14
R2	PRE BAKE			54.1	60.7	63.6	66.6	66.5	69.8	69.4	68.7	33.2		
	POST BAKE			50.5	57.1	60.1	63.1	62.9	66.6	66.2	65.8	30.1		
	DELTA (%)			-6.65	-5.93	-5.50	-5.26	-5.41	-4.58	-4.61	-4.22	-9.34		
R3	PRE BAKE		50.7	58.7		71.6	72.9	76.5	77.1	76.2	70.6	63.4	63.6	51
	POST BAKE		47.3	55.2		68.1	69.5	73.2	73.8	73.1	67.5	60.4	60	58
	DELTA (%)		-6.71	-5.96		-4.89	-4.66	-4.31	-4.28	-4.07	-4.39	-4.73	-5.66	13.73
R4	PRE BAKE	49.3	58.8	56.7	69.6	71.4	76.4	78.5	77.6	78.4	74.1	64.3	62.5	58.6
	POST BAKE	45.8	55.7	53.2	66.3	68.3	73.2	75.3	74.3	75.3	70.5	61.1	59.3	55.3
	DELTA (%)	-7.10	-5.27	-6.17	-4.74	-4.34	-4.19	-4.08	-4.25	-3.95	-4.86	-4.98	-5.12	-5.63
R5	PRE BAKE	56.3	61.6	69	70.5	70	74.5	75.7	77.3	75	67.3	63.1	61.4	59.1
	POST BAKE	52.5	57.9	65.5	67.3	66.8	71.4	72.8	74.1	71.8	64.4	60	58.2	55.6
	DELTA (%)	-6.75	-6.01	-5.07	-4.54	-4.57	-4.16	-3.83	-4.14	-4.27	-4.31	-4.91	-5.21	-5.92
R6	PRE BAKE	52.8	56.2	66.2	71.7	69.4	68.9	70.4	70.7	70.8	70.6	66.8	61.9	
	POST BAKE	49.3	52.7	62.8	68.8	66.1	65.9	67.4	67.6	67.3	67.3	63.1	58.4	
	DELTA (%)	-6.63	-6.23	-5.14	-4.04	-4.76	-4.35	-4.26	-4.38	-4.94	-4.67	-5.54	-5.65	
R7	PRE BAKE			61.8	65.8	65.1	63.6	66.4	66.7	66.2	66.9	61.2		
	POST BAKE			58.3	62.3	61.6	60.3	63.3	63.6	63	63.6	57		
	DELTA (%)			-5.66	-5.32	-5.38	-5.19	-4.67	-4.65	-4.83	-4.93	-6.86		
	AVERAGE	-4.83 %												

Figure 15. Summary of Stabake Deltas of OWR-4 Lot

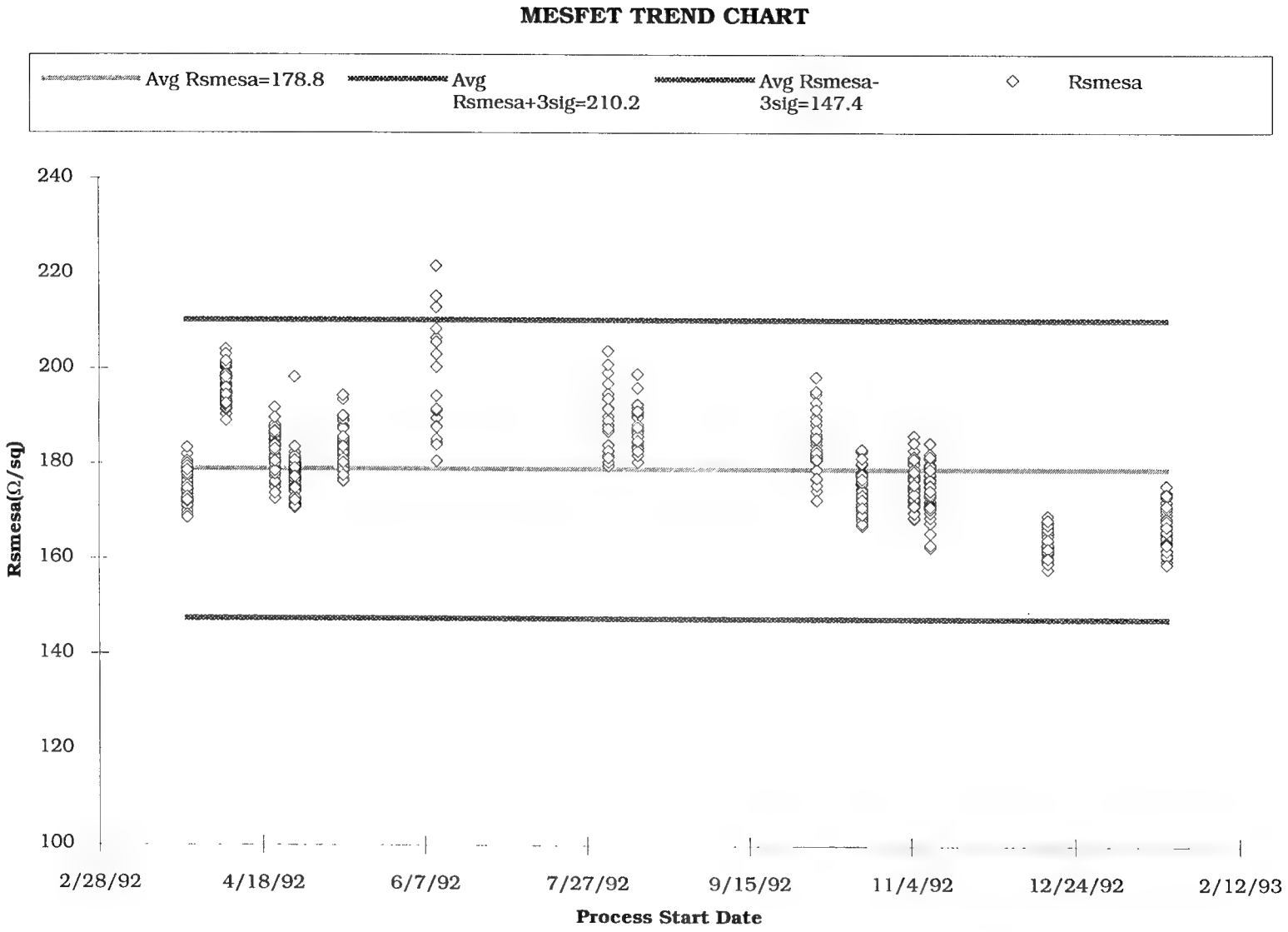


Figure 16. MESFET Trend Chart

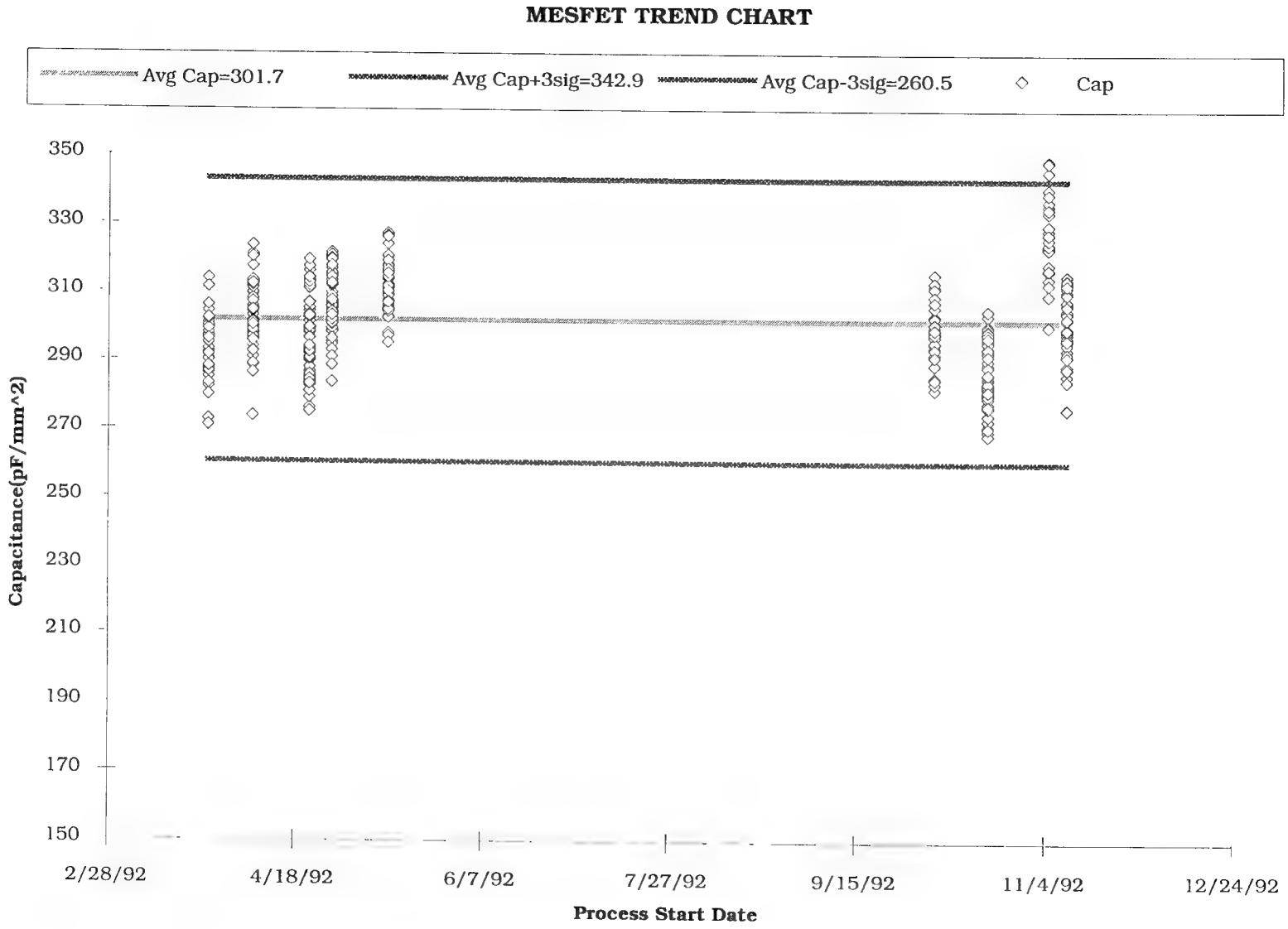


Figure 17. MESFET Trend Chart

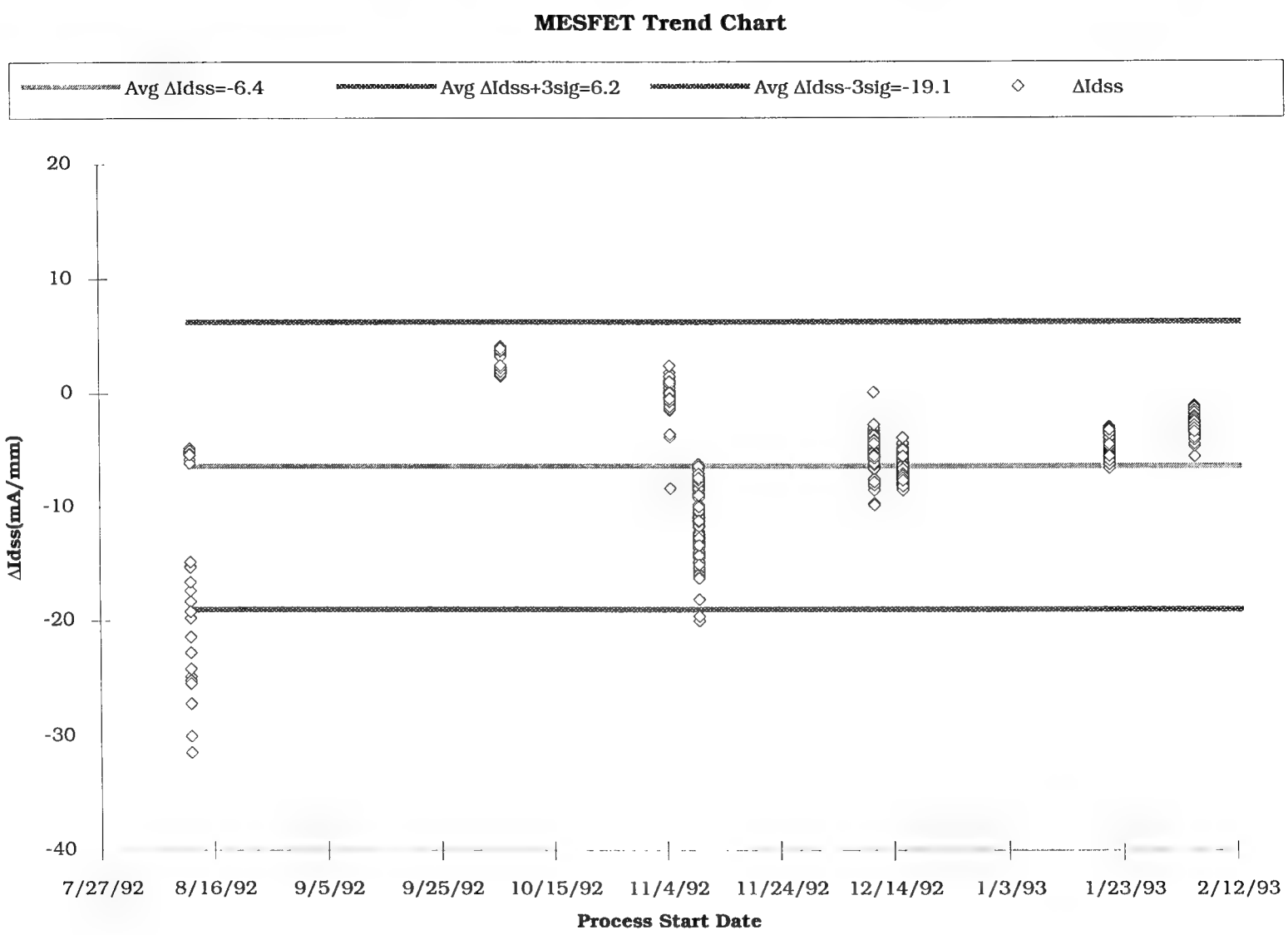


Figure 18. MESFET Trend Chart

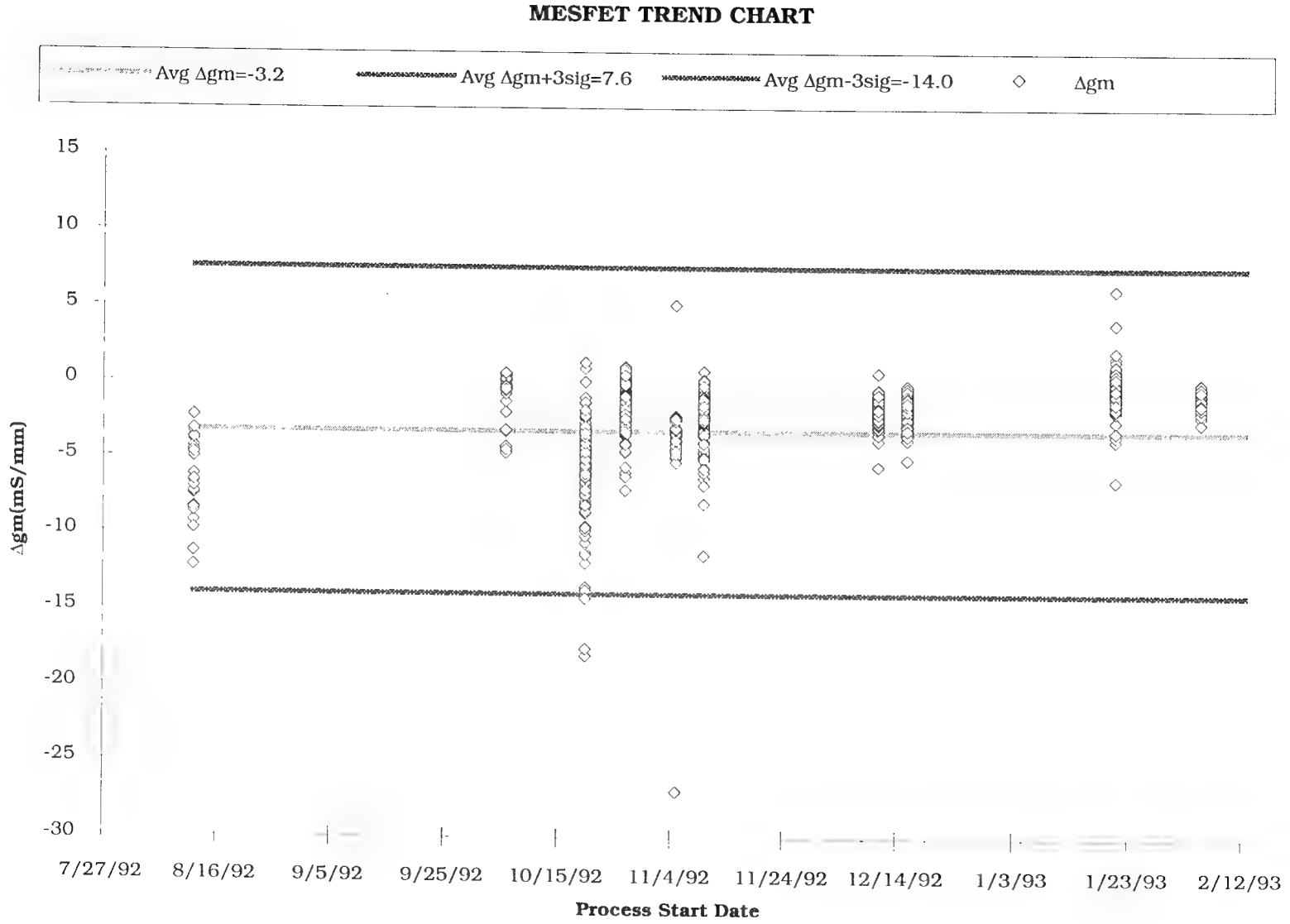


Figure 19. MESFET Trend Chart

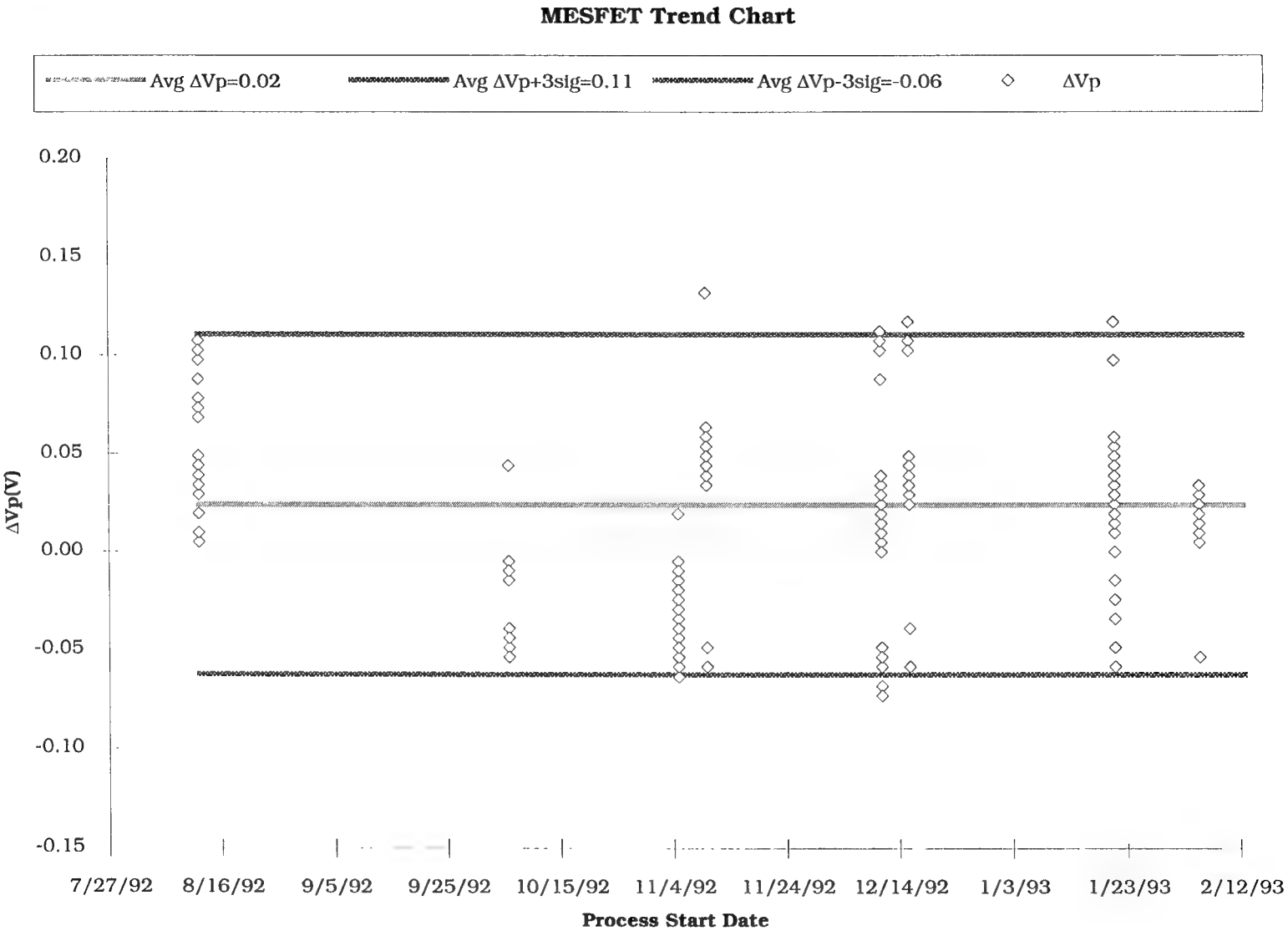


Figure 20. MESFET Trend Chart

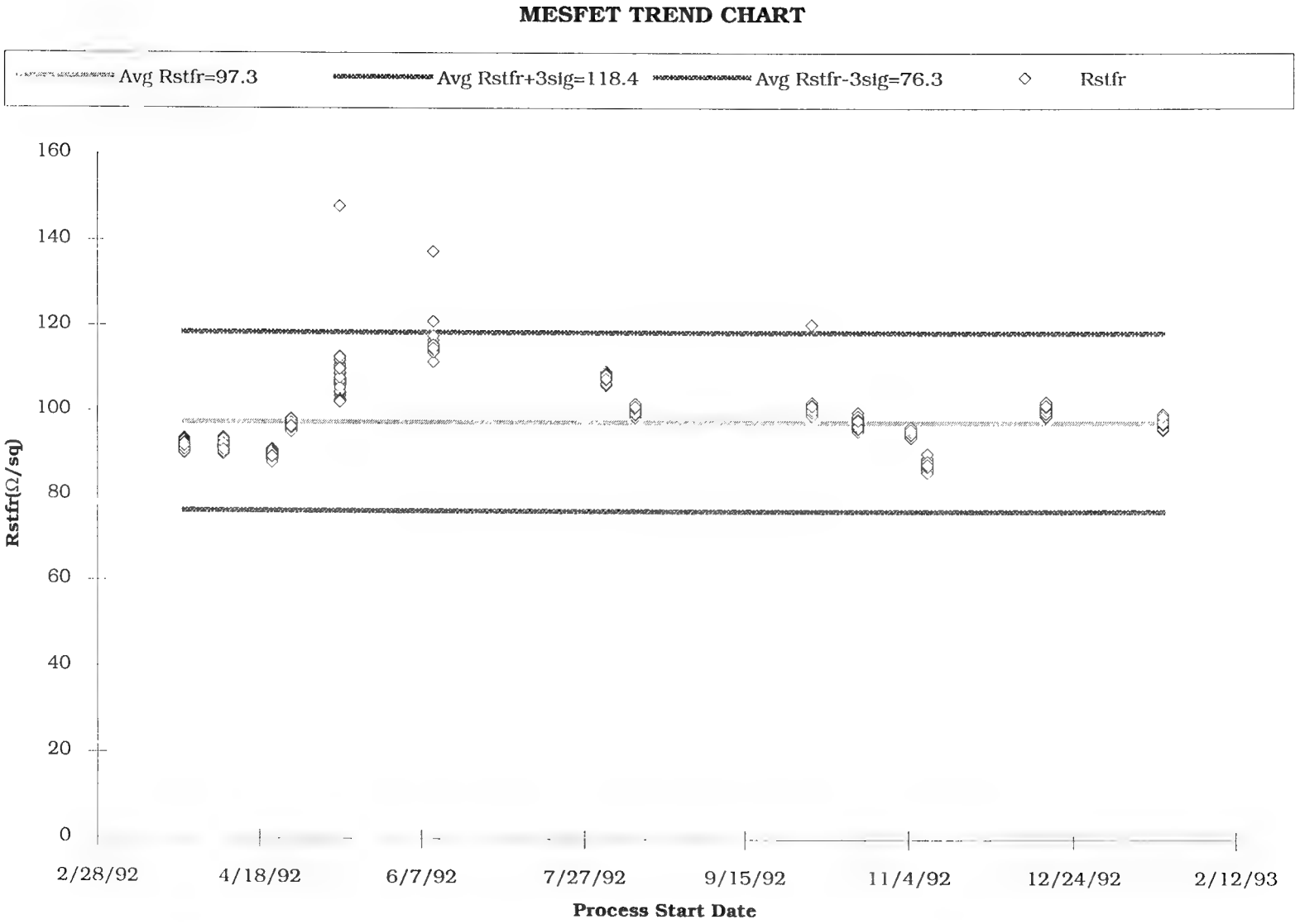


Figure 21. MESFET Trend Chart

action item. If the parameter exceeds the limit on one isolated case, the process will continue, however explanation is required to the ICAB for being out of specification.

2.1.5 Wafer Fabrication Yield

TRW's new GaAs manufacturing line has been in operational since 1988; and full production of MESFET, low noise HEMT, high linearity HEMT, Power HEMT, microwave HBT and digital HBT, etc., all started in 1991. Qualification of GaAs manufacturing line was initiated in early 1992. The wafer processing (OWR-1 and 2) for "Techniques for on-wafer reliability testing for MMICs (OWR)" was performed just before the qualification lots. For wafer fabrication yield analysis, we included all the lots fabricated from early 1992 to the first quarter of 1993; with most of MESFETs being fabricated for various programs. Figure 22 summarizes the MESFET lots fabricated in GaAs manufacturing line in D1. An average wafer yield is 75%. The earliest four lots had zero yield due to a possible metal contamination problem. The remaining 42 lots had 82% yield. Most of the wafer loss is due to wafer breakage during the backside process. A few lots described in Figure 22 had in-process problems. Overall the wafer fabrication yield improved significantly in the last two years, particularly in backside processing.

2.1.6 On-wafer RF Testing of SECs

On-wafer DC/RF evaluation of SECs was performed using HP 8510C with standard testing software for s-parameter measurements. Figure 23 shows s-parameter of one of the DAs in OWR-4, 206-067A wafer. The input and output return losses of -20.2 (specification is -11 dB) and -16.9 dB (specification is -11 dB), respectively are recorded. The Isolation was over 31 dB (specification is 20 dB). Figure 24 shows a summary of DC/RF parameters evaluated at wafer level. The small signal gain of OWR-4 lot is highly consistent compared to the previous flight production lots (gain values ranged 2.5 - 4.6 dB).

LOT No.	PRODUCT	Description	Project	Start date	Cmpl date	Started	Compltd	Line Yield	Comments
MHCTS-D27	MHCTS	MIMIC DEMO #2	MIMIC	3/24/93	5/20/93	6	6	100%	
MHCTS-D26	MHCTS	MIMIC DEMO #2	MIMIC	3/22/93	5/19/93	6	5	83%	
MHCTS-D25	MHCTS	MIMIC DEMO #2	MIMIC	3/17/93	5/18/93	6	5	83%	
MHCTS-D23	MHCTS	MIMIC DEMO #2	MIMIC	3/10/93	5/5/93	6	5	83%	
MHCTS-D24	MHCTS	MIMIC DEMO #2	MIMIC	3/15/93	5/5/93	6	6	100%	
MHCTS-D22	MHCTS	MIMIC DEMO #2	MIMIC	3/8/93	4/28/93	6	6	100%	
MHCTS-D21	MHCTS	MIMIC DEMO #2	MIMIC	3/3/93	4/21/93	6	5	83%	
MHCTS-D19	MHCTS	MIMIC DEMO #2	MIMIC	2/24/93	4/9/93	6	6	100%	
MHCTS-D20	MHCTS	MIMIC DEMO #2	MIMIC	3/1/93	4/9/93	6	4	67%	
MHCTS-D18	MHCTS	MIMIC DEMO #2	MIMIC	1/27/93	4/7/93	6	6	100%	
MHCTS-34	MHCTS	QUAL BACKUP	PM&P	11/5/92	3/24/93	6	6	100%	
MHCTS-36	MHCTS	BACKUP QUAL	PM&P	12/16/92	3/24/93	6	6	100%	
MHCTS-30	MHCTS	QUAL BACKUP	PM&P	10/20/92	3/10/93	6	5	83%	
OWR-4	OWR	DA QUAL	PM&P	7/22/92	12/7/92	6	6	100%	
OWR-5	OWR	RELIAB. EVAL	PM&P	8/12/92	11/25/92	5	4	80%	
THF1-3	THF1	Brassboard	MIMIC	3/5/92	11/4/92	6	6	100%	
AMXD-3	AMXD	R6/D1 Compariso	PM&P	6/10/92	10/30/92	4	3	75%	
PSC2-4	PSC2	R6/D1 Compariso	PM&P	6/16/92	9/22/92	6	5	83%	
WCSM-3	WCSM	R6/D1 Compariso	PM&P	6/30/92	9/22/92	6	5	83%	
PFS2-3	PFS2	R6/D1 Compariso	PM&P	6/11/92	8/28/92	6	4	67%	
MHCTS-12	MHCTS/P	Qualification Lot	PM&P	4/22/92	7/27/92	6	5	83%	
MHCTS-13	MHCTS/P	Qualification Lot	PM&P	4/28/92	7/27/92	6	3	50%	
MHCTS-11	MHCTS/P	Qualification Lot	PM&P	4/15/92	7/22/92	6	2	33%	
MHCTS-14	MHCTS/P	Qualification Lot	PM&P	5/13/92	7/16/92	6	0	0%	Failed BVgsx
THF1-4	THF1	Brassboard	MIMIC	3/11/92	7/15/92	6	5	83%	
MHCTS-9	MHCTS/P	Qualification Lot	PM&P	3/19/92	7/15/92	6	4	67%	
MHCTS-10	MHCTS/P	Qualification Lot	PM&P	3/26/92	7/14/92	6	5	83%	
MHCTS-D16	MHCTS	Demo	MIMIC	2/13/92	4/8/92	6	4	67%	
MHCTS-D13	MHCTS	Demo	MIMIC	2/10/92	4/7/92	6	6	100%	
MHCTS-D17	MHCTS	Demo	MIMIC	2/17/92	4/7/92	6	4	67%	
MHCTS-D15	MHCTS	Demo	MIMIC	2/12/92	4/6/92	6	5	83%	
MHCTS-D3	MHCTS	Demo	MIMIC	1/23/92	3/30/92	6	5	83%	
MHCTS-D9	MHCTS	Demo	MIMIC	2/3/92	3/30/92	6	5	83%	
MHCTS-D12	MHCTS	Demo	MIMIC	2/6/92	3/30/92	6	5	83%	
MHCTS-D14	MHCTS	Demo	MIMIC	2/11/92	3/30/92	6	3	50%	Wrong Ω thickness
MHCTS-D7	MHCTS	Demo	MIMIC	1/29/92	3/26/92	6	6	100%	
MHCTS-D2	MHCTS	Demo	MIMIC	1/22/92	3/24/92	6	6	100%	
MHCTS-D4	MHCTS	Demo	MIMIC	1/24/92	3/24/92	6	5	83%	
MHCTS-D5	MHCTS	Demo	MIMIC	1/27/92	3/24/92	6	6	100%	
MHCTS-D10	MHCTS	Demo	MIMIC	2/4/92	3/20/92	6	5	83%	
MHCTS-D6	MHCTS	Demo	MIMIC	1/28/92	3/17/92	6	6	100%	
MHCTS-D1	MHCTS	Demo	MIMIC	1/21/92	3/9/92	6	5	83%	
MHCTS-D11	MHCTS	Demo	MIMIC	2/5/92	2/24/92	6	0	0%	Scrapped at SiN, low BVgsx
MHCTS-D8	MHCTS	Demo	MIMIC	1/30/92	2/19/92	6	0	0%	Baked at High Temp at PR
OWR-1	OWR/P	On-Wafer Reliabili	OWR	1/10/92		6	0	0%	Δldss @ Stabake
OWR-2	OWR/P	On-Wafer Reliabili	OWR	2/3/92		6	0	0%	Δldss @ Stabake
Average								75.%	

Figure 22. Summary of Wafer Yield of MESFET MMICs in D1 Manufacturing Line

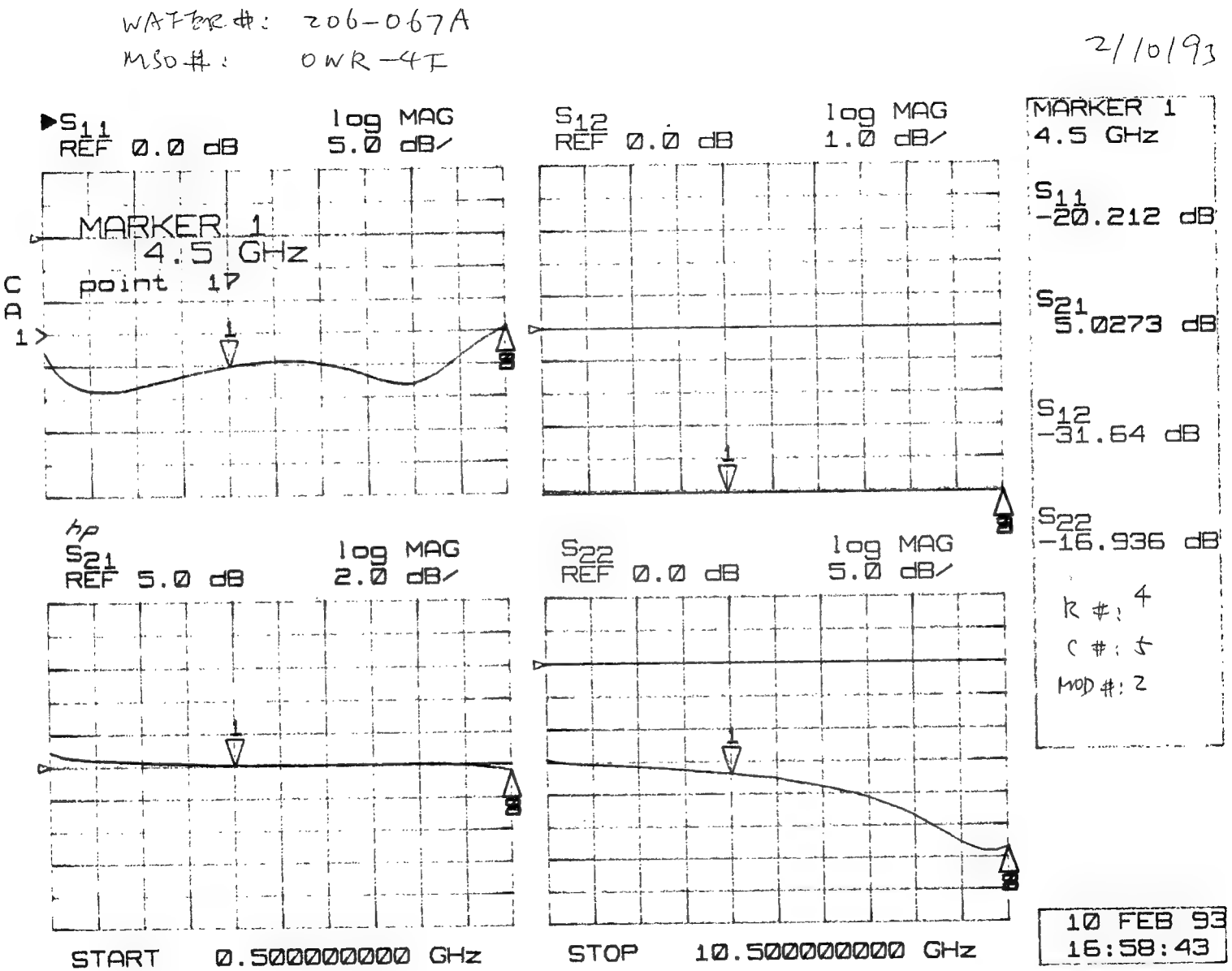


Figure 23. S-Parameters of OWR-4, On-Wafer Measurements

OWR-4, Wafer No: 206-66A Vdd=4.5V F=4.5GHz								
Row	Column	MOD	Idss (mA)	Vg at 0.5 Id	S21 (dB)	S11(dB)	S22 (dB)	Comment
2	2	2						Short
		3						Short
		1						Short
2	3	2	113.3	-0.553	4.9	-24.3	-17	
		3	119	-0.579	4.84	-24.5	-16.7	
		1	115.7	-0.56	4.86	-24	-16.9	
2	4	2	129.2	-0.63	4.79	-24	-16.7	
		3	134.9	-0.67	4.73	-24	-16.7	
		1	129	-0.63	4.82	-24	-16.7	
2	5	2	133.5	-0.67	4.66	-24	-16.6	
		3	134.3	-0.668	4.69	-24	-16.5	
		1	128.9	-0.62	4.77	-23.9	-16.5	
2	6	2	134.2	-0.67	4.67	-23.9	-16.6	
		3	135.9	-0.678	4.65	-23.9	-16.5	
		1	133	-0.655	4.72	-24.2	-16.5	
2	7	2	141.9	-0.71	4.62	-24	-16.5	
		3	143.4	-0.72	4.62	-24.1	-16.5	
		1	143.8	-0.72	4.64	-23.9	-16.4	
2	8	2	146.5	-0.755	4.52	-24.2	-16.4	
		3	148.4	-0.755	4.51	-24	-16.4	
		1	145.3	-0.729	4.61	-24	-16.4	
2	9	2	150.6	-0.774	4.52	-24.1	-16.4	
		3	149.9	-0.76	4.57	-24.1	-16.4	
		1	147.1	-0.736	4.62	-24.3	-16.3	
2	10	2	149	-0.75	4.62	-24.5	-16.4	
		3	146.4	-0.73	4.71	-24.9	-16.4	
		1	145	-0.72	4.76	-24.4	-16.4	
2	11	2	141.1	-0.695	4.72	-24.2	-16.4	
		3	137.9	-0.668	4.85	-24.7	-16.5	
		1	133.9	-0.64	4.87	-24.9	-16.8	
2	12	2	130	-0.624	4.9	-24.9	-16.5	
		3	128	-0.61	4.96	-24.9	-16.6	
		1	129.2	-0.71	2.99	-22.2	-15.9	
2	13	2						Short
		3	119.9	-0.56	4.35	-27.1	-16.2	
		1	114.7	-0.53	5	-24.8	-16.9	
	AVERAGE		139.77	-0.69	4.81	-25.06	-17.05	

Figure 24. Summary of DC/RF Parameters of OWR-4, On-Wafer

OWR-4, Wafer No: 206-66A Vdd=4.5V F=4.5GHz								
Row	Column	MOD	Idss (mA)	Vg at 0.5 Id	S21 (dB)	S11(dB)	S22 (dB)	Comment
3	1	2						Short
		3						Short
		1						Short
3	2	2	111.3	-0.522	4.84	-25.3	-17.2	
		3	114.4	-0.561	4.82	-25.6	-17.2	
		1	113.3	-0.561	4.81	-25.5	-17.2	
3	3	2	119.4	-0.598	4.71	-25.8	-17.1	
		3	121.3	-0.612	4.73	-25.9	-17.2	
		1	120.1	-0.589	4.74	-25.8	-17	
3	4	2	129.4	-0.653	4.59	-25.6	-17	
		3	131.4	-0.681	4.51	-25.7	-16.9	
		1	133.7	-0.685	4.56	-25.5	-16.9	
3	5	2	137.2	-0.725	4.43	-25.7	-16.9	
		3	140.9	-0.737	4.4	-25.7	-16.8	
		1	142.1	-0.75	4.38	-25.4	-16.7	
3	6	2	144.3	-0.764	4.37	-25.3	-16.8	
		3	141.9	-0.72	4.4	-25.7	-16.8	
		1	140.9	-0.72	4.38	-25.4	-16.7	
3	7	2	150.6	-0.781	4.61	-28.4	-17.4	
		3	147.5	-0.765	4.64	-28.4	-17.4	
		1	146.5	-0.758	4.66	-28.3	-17.4	
3	8	2	151.5	-0.81	4.52	-28.3	-17.4	
		3	153.9	-0.82	4.5	-28.6	-17.4	
		1	149.6	-0.81	4.49	-28.7	-17.3	
3	9	2	159.2	-0.84	4.57	-28.3	-17.4	
		3	157.9	-0.83	4.6	-28.5	-17.4	
		1	155	-0.805	4.63	-28.6	-17.4	
3	10	2	147.8	-0.758	4.7	-28.6	-17.4	
		3	137.8	-0.69	4.79	-28.8	-17.7	
		1						
3	11	2	150.8	-0.78	4.69	-28.3	-17.5	
		3	150.1	-0.775	4.73	-28.5	-17.2	
		1	147	-0.749	4.73	-28.9	-17.4	
3	12	2	141.6	-0.685	4.78	-25.2	-16.6	
		3	137.9	-0.65	4.85	-25.7	-16.5	
		1	138.2	-0.64	4.85	-25.5	-16.5	
3	13	2	123.5	-0.588	4.92	-25.7	-16.8	
		3	117.4	-0.553	5	-25.7	-16.8	
		1	121.6	-0.578	4.96	-25.7	-16.7	
3	14	2	118.1	-0.55	4.99	-25.1	-16.9	
		3	114.5	-0.54	4.91	-25.2	-16.9	
		1	112.3	-0.521	4.96	-25.2	-16.9	
	AVERAGE		139.78	-0.71	4.80	-27.35	-17.53	

Figure 24. Summary of DC/RF Parameters of OWR-4, On-Wafer (Continued)

OWR-4, Wafer No: 206-66A Vdd=4.5V F=4.5GHz								
Row	Column	MOD	Idss (mA)	Vg at 0.5 Id	S21 (dB)	S11(dB)	S22 (dB)	Comment
4	2	2	107.6	-0.531	4.66	-25.5	-17.3	
		3	109.7	-0.568	4.81	-28.2	-17.2	
		1	113.9	-0.55	4.76	-25.9	-17.2	
4	3	2	122.1	-0.602	4.65	-26	-17	
		3	123.9	-0.633	4.61	-25.9	-17.1	
		1	125.2	-0.629	4.6	-26.3	-16.9	
4	4	2	133.4	-0.737	4.54	-28.4	-16.9	
		3	132.2	-0.703	4.42	-25.9	-16.9	
		1	134.5	-0.713	4.38	-25.2	-16.8	
4	5	2	134.2	-0.692	4.45	-26.3	-16.9	
		3	135.5	-0.726	4.35	-26.3	-16.8	
		1	139.1	-0.734	4.37	-26.7	-16.7	
4	6	2	140.3	-0.716	4.36	-26.3	-16.8	
		3	139.8	-0.755	4.25	-26.4	-16.8	
		1	142.6	-0.769	4.29	-26.6	-16.8	
4	7	2	143.3	-0.774	4.22	-26.3	-16.8	
		3	143.9	-0.782	4.18	-26.2	-16.8	
		1	149.7	-0.8	4.12	-26.7	-16.7	
4	8	2	148.9	-0.84	4.14	-26.3	-16.8	
		3	150.1	-0.837	4.13	-26.4	-16.7	
		1	152.8	-0.836	4.16	-26.3	-16.6	
4	9	2	148.3	-0.786	4.27	-26.1	-16.7	
		3						Short
		1						Short
4	10	2	134	-0.753	4.43	-26.8	-16.7	
		3	139.3	-0.714	4.44	-26.9	-16.7	
		1	141.6	-0.726	4.41	-26.4	-16.6	
4	11	2	138.4	-0.735	4.42	-26.1	-16.7	
		3	139.7	-0.725	4.45	-25.9	-16.8	
		1	143.6	-0.738	4.4	-25.8	-16.7	
4	12	2	139.7	-0.735	4.48	-26.1	-16.8	
		3	136.7	-0.715	4.5	-26.3	-16.8	
		1	137.9	-0.74	4.51	-25.8	-16.8	
4	13	2	118.8	-0.602	4.65	-26.2	-16.8	
		3	114.4	-0.56	4.74	-25.9	-17	
		1	115.4	-0.569	4.75	-26.33	-16.9	
AVERAGE			134.43	-0.71	4.44	-26.32	-16.84	

Figure 24. Summary of DC/RF Parameters of OWR-4, On-Wafer (Continued)

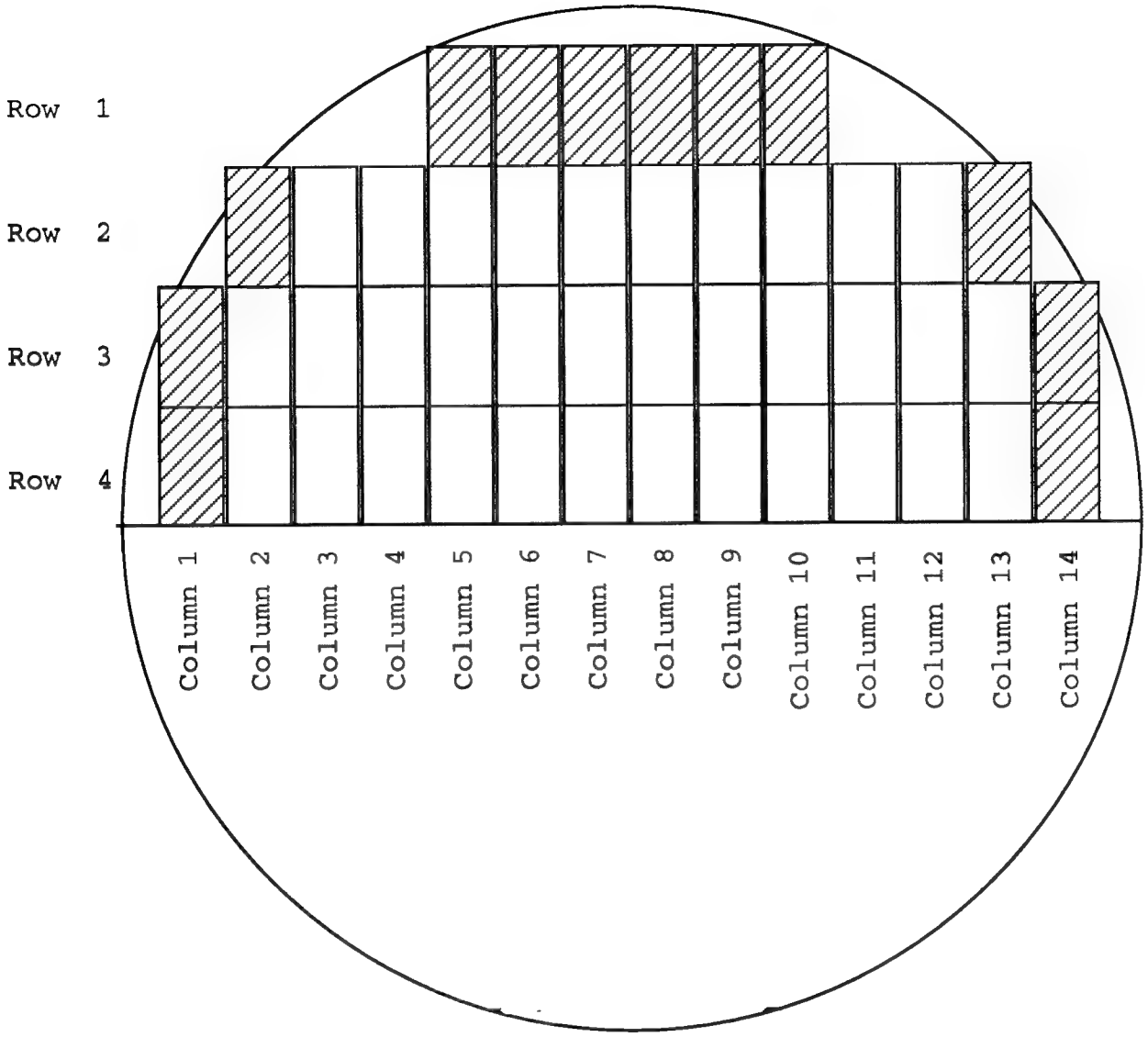
2.2 COMPLIANT INTERCONNECT STRUCTURE (CIS) DESIGN AND FABRICATION

2.2.1 CIS Design

The CIS was designed based on the MMIC mask layout. In accordance with the SOW, we designed the CIS on half a wafer to correlate between on-wafer and packaged MMIC reliability characteristics. There are 34 reticles per half wafer as shown in Figure 25. However due to limitation on the number of bias lines, (physical constraint to 100 dc bias lines per wafer because of ceramic connectors per life test fixture) we selected a total of 12 reticles for the dc bias life test. For statistical consideration, reticles were picked evenly throughout a half wafer as shown in Figure 26. Each reticle consists of two types of SECs: four distributed amplifiers (one is designed for on-wafer life testing and three for packaged SEC life test), two three-stage amplifiers (one is designed for on-wafer life testing); and six types of TCVs: one-air bridge metal, one-top metal, one-gate metal, one-ohmic contact, two-thin film resistors, and one-via-to-via. Figure 27 depicts CIS contact ID number and SEC/TCVs. Due to a limited number of contact lines, backside via TCV is inserted only into reticle B1, B2 and C1, C2 replacing top metal and gate metal. Other TCVs are in all reticles. For simpler fabrication process, we designed the CIS using a single layer interconnect, however, the bias line layout was complicated as shown in Figure 28.

2.2.2 Preliminary CIS Fabrication Using Kapton Polyimide

TRW's approach for on-wafer reliability testing technique was to use COIN technology. For this program it was renamed, Compliant Interconnect Structure (CIS). Our approach is to build inter connect layer deposit on Kapton polyimide (KAPTON Type VN Film made by Dupont), coat liquid polyimide (Dupont PI 2611), open the via hole by dry etch, then plate the contact bumps. Preliminary work on the CIS process development was performed using 3.5 mil thick Kapton polyimide. The layout for the preliminary CIS process development is shown in Figure 29.



Note: SECs and TCVs in shaded area are not tested because they are too close to the edge.

Figure 25. Row and Column Designation of OWR Wafer

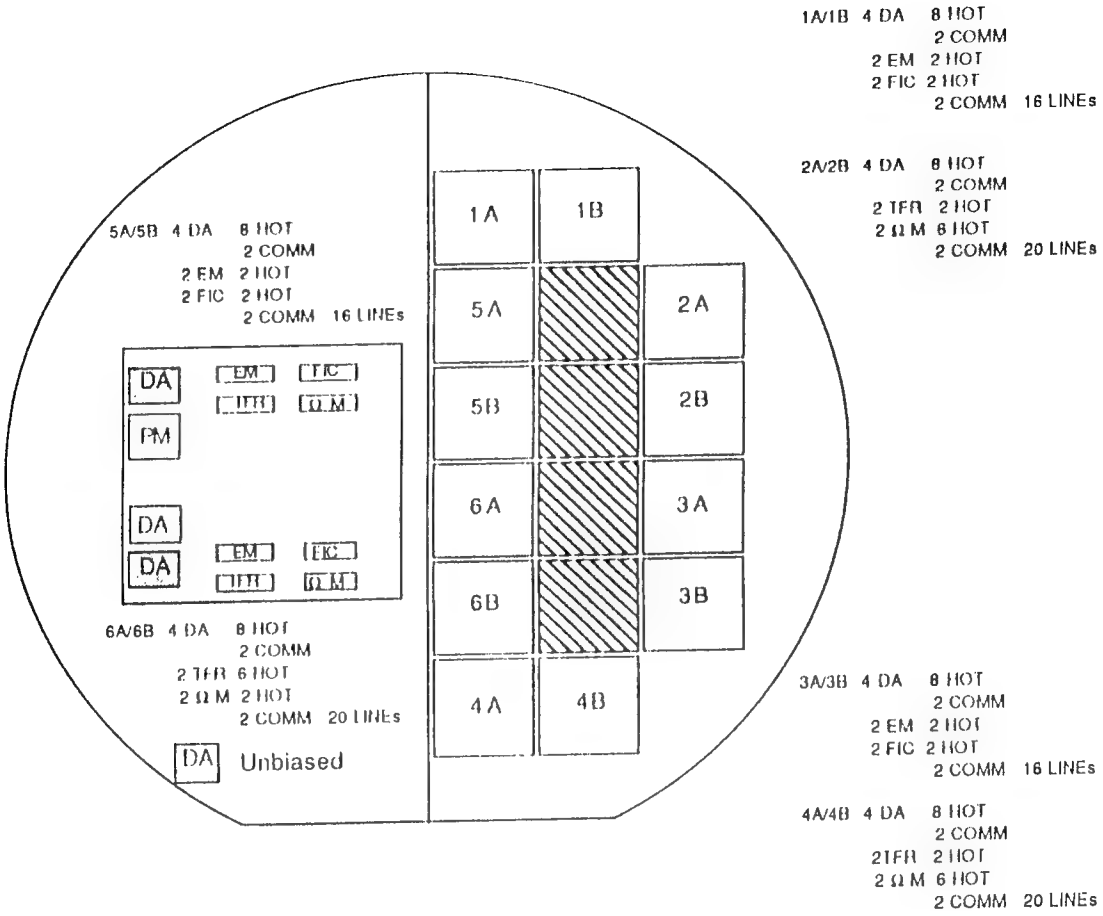


Figure 26. Preliminary MMIC Layout

CIS contact ID No.	Reticle No.	SEC/TCV ID.
A1	A1-1	DA-G
A2	A1-2	DA-D
A3	A1-3	XBC1-D
A4	A1-4	XBC1-G
A5	A1-5	Air bridge-hot
A6	A1-6	TM-hot
A7	A1-7	Gate metal-hot
A8	A1-8	Ohmic metal-hot
A9	A1-9	TFR-1
A10	A1-10	TFR-2
A11	A2-1	DA-G
A12	A2-2	DA-D
A13	A2-3	XBC1-G
A14	A2-4	XBC1-D
A15	A2-5	Air bridge-hot
A16	A2-6	TM-hot
A17	A2-7	Gate metal-hot
A18	A2-8	Ohmic metal-hot
A19	A2-9	TFR-1
A20	A2-10	TFR-2
B1	B1-1	DA-G
B2	B1-2	DA-D
B3	B1-3	XBC1-G
B4	B1-4	XBC1-D
B5	B1-5	Air bridge-hot
B6	B1-6	Via-hot
B7	B1-7	Via-ground
B8	B1-8	Ohmic metal-hot
B9	B1-9	TFR-1
B10	B1-10	TFR-2
B11	B2-1	DA-G
B12	B2-2	DA-D
B13	B2-3	XBC1-G
B14	B2-4	XBC1-D
B15	B2-5	Air bridge-hot
B16	B2-6	Via-hot
B17	B2-7	Via-ground
B18	B2-8	Ohmic metal-hot
B19	B2-9	TFR-1
B20	B2-10	TFR-2

Figure 27. CIS Identification and Reticle Numbers for SECs and TCVs

CIS contact ID No.	Reticle No.	SEC/TCV ID.
C1	C1-1	DA-G
C2	C1-2	DA-D
C3	C1-3	XBC1-G
C4	C1-4	XBC1-D
C5	C1-5	Air bridge-hot
C6	C1-6	Via-hot
C7	C1-7	Via-ground
C8	C1-8	Ohmic metal-hot
C9	C1-9	TFR-1
C10	C1-10	TFR-2
C11	C2-1	DA-G
C12	C2-2	DA-D
C13	C2-3	XBC1-G
C14	C2-4	XBC1-D
C15	C2-5	Air bridge-hot
C16	C2-6	Via-hot
C17	C2-7	Via-ground
C18	C2-8	Ohmic metal-hot
C19	C2-9	TFR-1
C20	C2-10	TFR-2
D1	D1-1	DA-G
D2	D1-2	DA-D
D3	D1-3	XBC1-G
D4	D1-4	XBC1-D
D5	D1-5	Air bridge-hot
D6	D1-6	TM-hot
D7	D1-7	Gate metal-hot
D8	D1-8	Ohmic metal-hot
D9	D1-9	TFR-1
D10	D1-10	TFR-2
D11	D2-1	DA-G
D12	D2-2	DA-D
D13	D2-3	XBC1-G
D14	D2-4	XBC1-D
D15	D2-5	Air bridge-hot
D16	D2-6	TM-hot
D17	D2-7	Gate metal-hot
D18	D2-8	Ohmic metal-hot
D19	D2-9	TFR-1
D20	D2-10	TFR-2

Figure 27. CIS Identification and Reticle Numbers for SECs and TCVs (Continued)

CIS contact ID No.	Reticle No.	SEC/TCV ID.
E1	E1-1	DA-G
E2	E1-2	DA-D
E3	E1-3	XBC1-G
E4	E1-4	XBC1-D
E5	E1-5	Air bridge-hot
E6	E1-6	TM-hot
E7	E1-7	Gate metal-hot
E8	E1-8	Ohmic metal-hot
E9	E1-9	TFR-1
E10	E1-10	TFR-2
E11	E2-1	DA-G
E12	E2-2	DA-D
E13	E2-3	XBC1-G
E14	E2-4	XBC1-D
E15	E2-5	Air bridge-hot
E16	E2-6	TM-hot
E17	E2-7	Gate metal-hot
E18	E2-8	Ohmic metal-hot
E19	E2-9	TFR-1
E20	E2-10	TFR-2
F1	F1-1	DA-G
F2	F1-2	DA-D
F3	F1-3	XBC1-G
F4	F1-4	XBC1-D
F5	F1-5	Air bridge-hot
F6	F1-6	TM-hot
F7	F1-7	Gate metal-hot
F8	F1-8	Ohmic metal-hot
F9	F1-9	TFR-1
F10	F1-10	TFR-2
F11	F2-1	DA-G
F12	F2-2	DA-D
F13	F2-3	XBC1-G
F14	F2-4	XBC1-D
F15	F2-5	Air bridge-hot
F16	F2-6	TM-hot
F17	F2-7	Gate metal-hot
F18	F2-8	Ohmic metal-hot
F19	F2-9	TFR-1
F20	F2-10	TFR-2

Figure 27. CIS Identification and Reticle Numbers for SECs and TCVs (Continued)

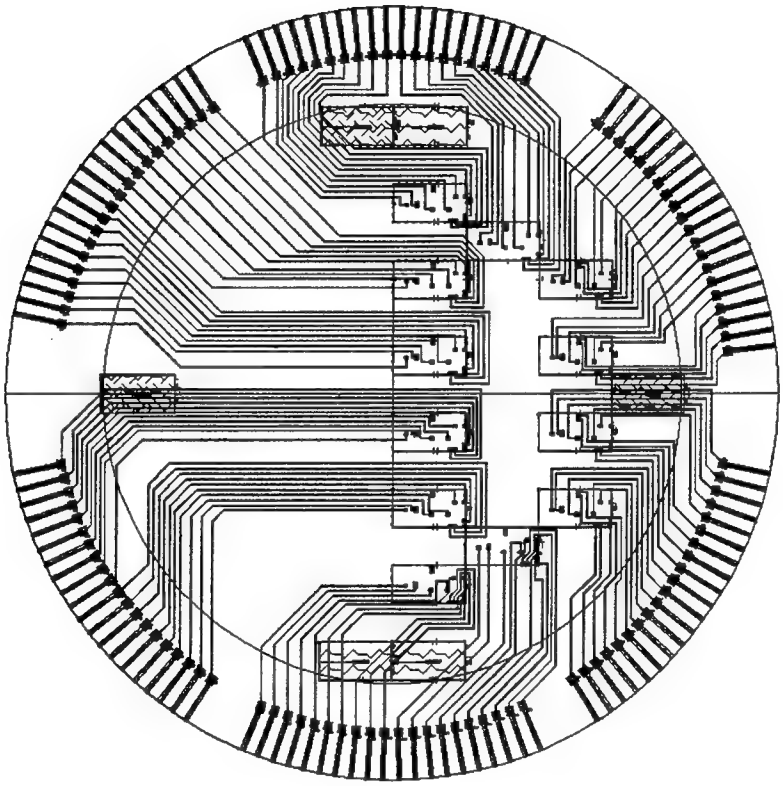


Figure 28. CIS Interconnect Metal Layer Design

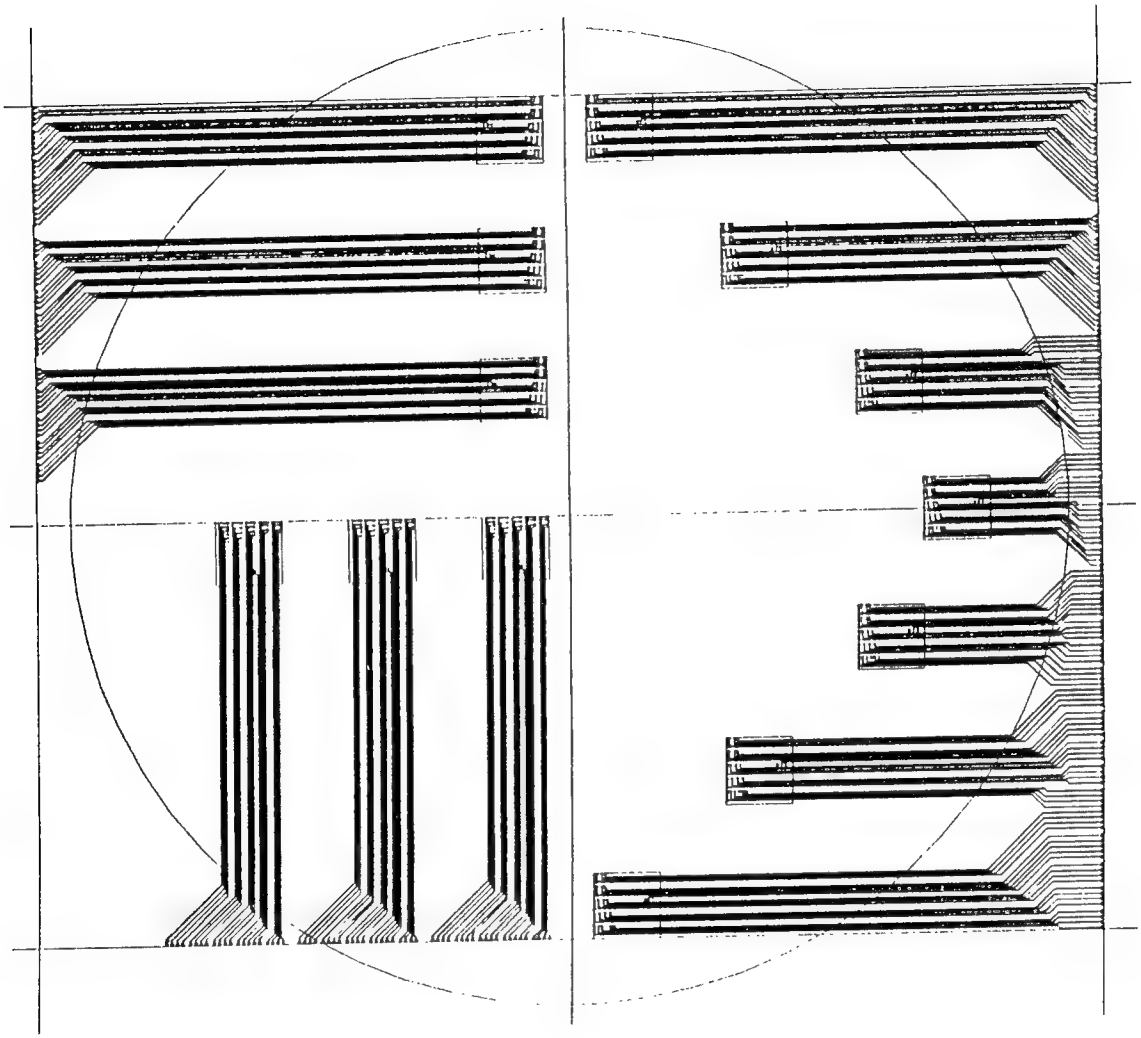


Figure 29. Preliminary CIS Study – Contact Bump Layout

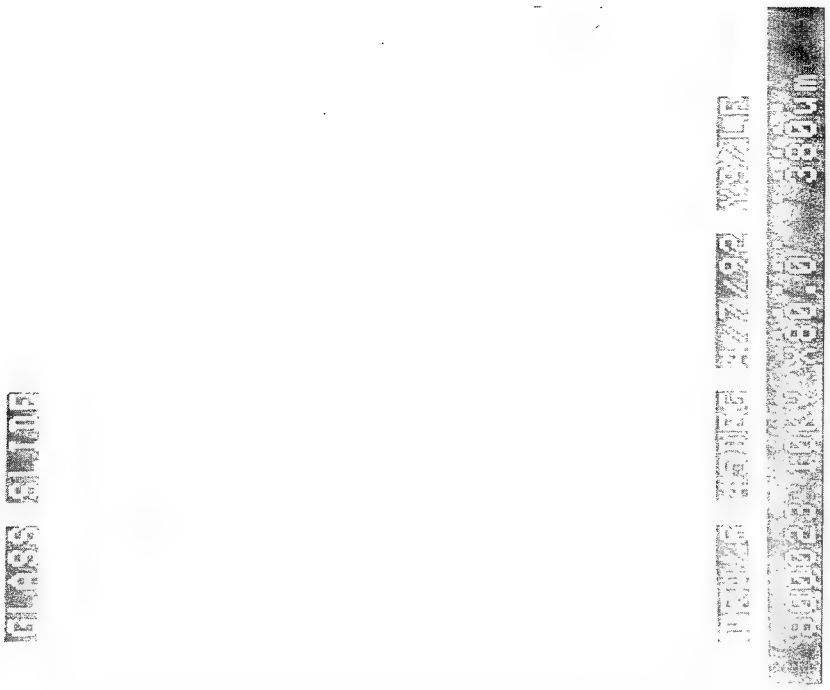
Because of stress created by the sputtered metals, the Kapton film curled. To alleviate this problem, we deposited metals on both sides to equalize stress. Although this method worked very well, the film curled again during the baking process while curing the liquid polyimide. The curling was not severe enough to terminate the processing. If the Kapton film could not to mount on flat carrier for coating photoresist, the further processing would have to be discontinued (described in section 2.2.4 for improved processing).

However, in photolithography for via hole formation, the interconnect and the via did not align -- particularly at the outer edge of 4 inch wafer. This misalignment is caused by shrinkage of Kapton substrate while curing the liquid polyimide. Largest displacement is approximately 100 μm at 1.5" from center of the wafer. To alleviate this problem, we decided to use borosilicate glass as substrate.

In via hole formation for contact bumps, we tried a plasma etching method using Technic II, however the dry etch was unsuccessful for glass because of the non conductive substrate. Excimer laser system was used to burn off the polyimide. Figure 30 shows via holes burnt off by a laser beam. As shown in the SEM micrographs, the polyimide was cleanly burnt off. This laser drilling was done by Applied Laser Technology, Inc. in Oregon.

2.2.3 CIS Fabrication with Glass Substrate

Borosilicate glass is selected as a substrate that has a thermal expansion coefficient similar to GaAs, and has higher mechanical strength. A 20 mil 3" glass wafer gives a reasonable compliancy across 3" wafer, thus we believed that ohmic contact between contact bumps of CIS and GaAs wafer would be good. The manufacturing shop order (MSO) for the CIS fabrication is shown in Figure 31. The CIS process flow diagram is shown in Figure 32.



a) CIS Contact Vias and Interconnect Lines

b) Close-up View of the CIS Via

Figure 30. SEM Micrographs of CIS Contact via Formation by Excimer Laser Process

CIS Manufacturing Shop Order 7/6/92

Part Description:_____ Job No.: 1C9770
MSO No.: _____ Wafer No.: _____
Part No. _____
Mask Set No.: _____

Step	MF1	Rev	Sect	Procedure	Comments	Qty	Badge	Date
				Lot Initiation (3864)				
0.1.0	3864			KIT wafers				
0.1.1				Wafer Identification				
				First Interconnect (3961)				
1.0.0 ⇓				Clean wafers	TCE/Acetone/Methanol, blow dry			
1.1.0 ⇓				Sputter FIC plating Medium	Ps ≤ 3.0 E-7 Torr Log No._____ Back Sputter Metal Thickness(Å) Rate(Å/sec) Cr 500 Au 2000			
1.1.1				Plate FIC	Thickness = 1.5µm			
1.1.2				Coat PR; KTI 1370SF Air Dry Prebake PR	3000rpm, 30 sec. 20 min. 95°C, 20 min.			
1.1.3				Expose/dev: Mask No.____ Mask SN:_____ Mask Rev:_____	MJB, 15 sec. @ ____mW/cm2 Microposit:DI (1:1), 1.5 min. Rinse, 1 min. Dry			
1.1.4				Workmanship Verification	Reprocess (circle one): Yes No			
1.2.0				Postbake	95°C, 20 min.			
1.2.1				Etch Au Etch Cr	FMI gold remover			
1.2.2				Strip PR	ACE			
1.2.3				Workmanship Verification				

Figure 31. CIS Manufacturing Shop Order 7/6/92

CIS Manufacturing Shop Order 7/6/92

Part Description:_____ Job No.: 1C9770
MSO No.: _____ Wafer No.: _____
Part No. _____
Mask Set No.: _____

Step	MF1	Rev	Sect	Procedure	Comments	Qty	Badge	Date
				Top Metal (3878)				
3.0.0				Clean	NH4OH:H2O (1:10), 15 sec Rinse 15 sec, dry			
3.1.1				Sputter Plating medium	Metal Thk(A) Ti 500 Au 1000 Ti 300			
3.1.2				Coat PR: AZ4620	1000rpm, 30 sec.			
3.1.3				Bake (Horizontal)	90°C, 30 min.			
3.1.4				Coat PR: AZ4620	1500rpm, 30 sec.			
3.1.5				Bake (Horizontal)	90°C, 60 min.			
3.1.6				Expose/dev: Mask No.____ Mask SN:_____ Mask Rev:_____	MJB, 3 min. @_____ mW/cm2 AZ400K:DI (1:4), 10 min. Rinse, 2 min. Dry			
3.1.7.				Workmanship Verification	Reprocess (Circle One): Yes No			
3.2.0				Measure PR Thickness	Dektak one site in center, one site at edge			
3.2.1				Descum	IPC, O2@0.2 Torr, 100W, 1 min.			
3.2.2				DUV Flood Exposure PR	HTG 345-10, 20 min. @____mW/cm2			
3.2.3				Etch Ti				
3.2.4				Plate Top Metal	Thickness = 25µm			
3.2.5				Workmanship Verification				
3.3.0				Evaporate Metal	Metal Thk(A) Rate(A/s) Pt 300			
3.3.1				Lift Off	ACE			
3.3.2				Measure Plated Gold thickness				
3.3.3				Etch Ti/Au/Ti				
3.3.4				Measure Top Metal thickness				

Figure 31. CIS Manufacturing Shop Order 7/6/92 (Continued)

CIS Manufacturing Shop Order 7/6/92

Part Description:_____
MSO No.: _____
Part No. _____
Mask Set No.: _____

Job No.: 1C9770
Wafer No.: _____

Step	MF1	Rev	Sect	Procedure	Comments	Qty	Badge	Date
				Polyimide				
2.0.0				Coat Adhesion Promoter VM651 Bake	5000rpm, 30 sec. Oven 100°C, 1 min.			
2.1.1				Coat PI2611 Bake	5000rpm, 30 sec. Oven 350°C, 1 hr.			
2.1.2				Evaporate Metal	Metal Thk(A) Rate(A/sec) Ti 500 Au 1000-			
2.1.3				Coat PR: KTI 1370SF Air Dry Prebake PR	3000rpm, 30sec 20 min. 95°C, 20 min.			
2.1.4				Expose/dev: Mask No.____ Mask SN:____ Mask Rev:____	MJB, 15 sec. @ _____mW/cm2 Microposit: DI (1:1), 1.5 min Rinse, 1 min. Dry			
2.1.5				Workmanship Verification	Reprocess (Circle one): Yes No			
2.2.0				Etch Au Etch Ti	Aurostrip			
2.2.1				Strip PR	ACE			
2.2.2				Workmanship Verification				
2.3.0				RIE Polyimide	Plasma Therm O2 flow 40 sccm O2 pressure 35 mTorr Power: 80 watts Time: 105 min.			
2.3.1				Workmanship Verification				
2.3.2				Strip Au Strip Ti	Aurostrip			
2.3.3				Workmanship Verification				

Figure 31. CIS Manufacturing Shop Order 7/6/92 (Continued)

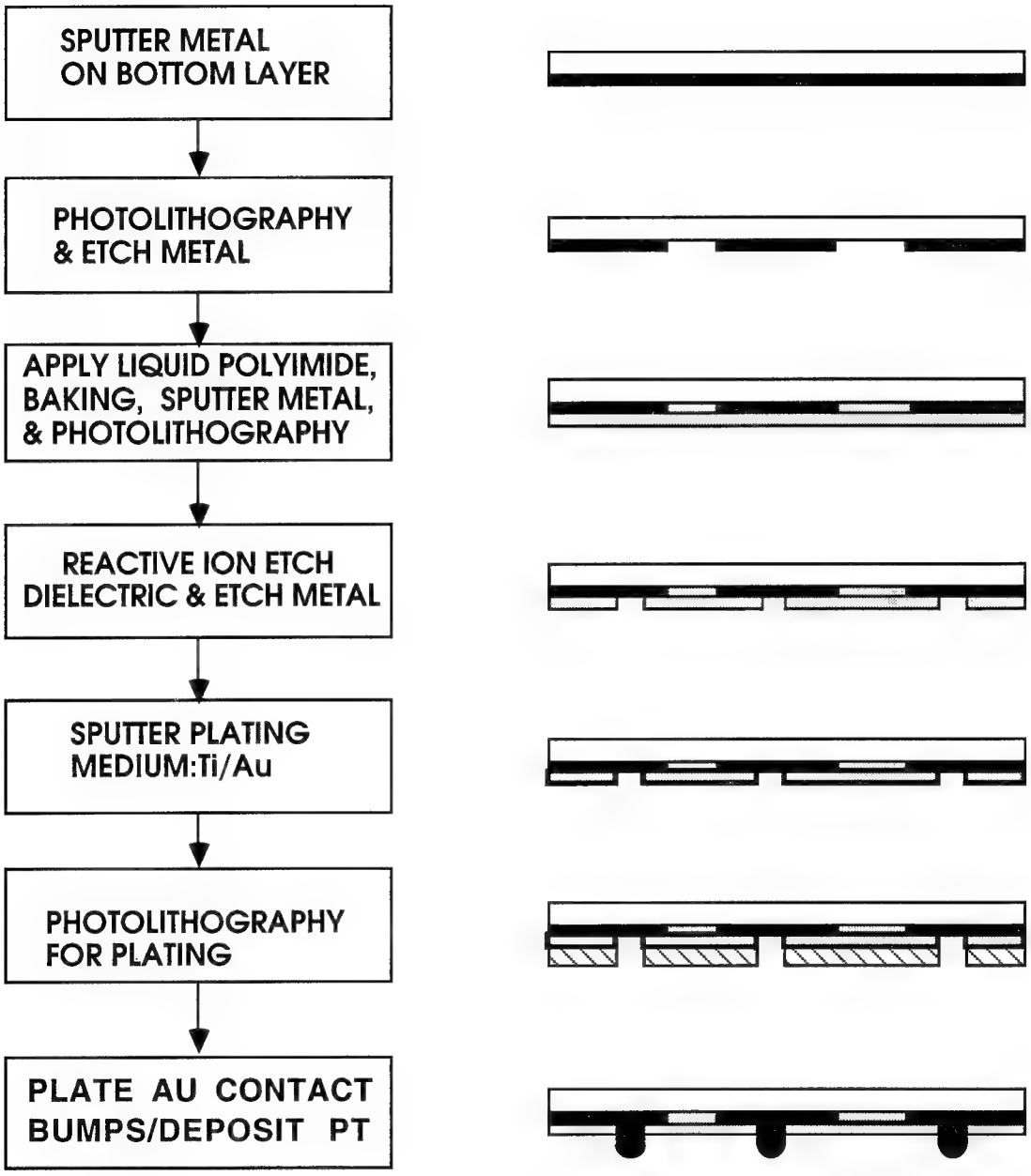


Figure 32. CIS Fabrication Process Flow Diagram

First Interconnect Layer Formation

The first interconnect metal layer (500Å Ti/1000Å Au) was deposited by an Innotec down sputter system. Additional 1.5μm thick gold was electroplated by pulse plating method. Through photolithography and etching process, the first interconnect layer was formed.

Dielectric Layer with Liquid Polyimide

An adhesion promoter VM651 was first coated on glass substrate and baked at 100°C for one minute. Then liquid polyimide (Dupont PI 2611) was coated by spinning at 5000 rpm for 30 seconds, and baked at 350°C for one hour. The adhesion promoter is necessary to enhance adhesion of liquid polyimide on the glass substrate, otherwise the coated polyimide peels off after the baking process that for cures the film.

Formation of Via Holes (Lift-off Method)

Although the Excimer laser is an excellent tool for the formation of clean via holes, a decision was made to use the reactive ion etch system for its availability in the GaAs manufacturing line at TRW.

We used Ti/Au as a mask for dry etch of via hole by reactive ion etch process. Through photolithography we opened square vias. The reactive ion etch condition had an oxygen flow rate of 40 SCCM, oxygen pressure of 35 mTorr, and power of 80 watts. The etching time was 105-110 minutes. This dry etch condition was optimized by experimenting on a few runs prior to the etching of real wafer. The dry etch was stopped when it reached the interconnect metal (Ti/Au) surface, thus actual time to etch 2μm polyimide is shorter than 105 min.

Plating Contact Bumps

After we examined the via holes for organic residues, we sputter deposited Ti/Au/Ti as a plating medium. By photolithography, the via holes were opened for gold plating. Prior to gold plating, we etch out the Ti layer (Ti layer act as protection film during process). Gold plating in via was conducted by pulse plating to ensure its excellent

height uniformity of the gold contact bumps. Typical wafer mapping for gold bumps is shown in Figure 33. A thin-film platinum layer was deposited by electron beam evaporator to prevent Au-Au from fusing during high temperature life test.

Deposition of Pt on Plated Au
To prevent Au-Au fusing during life test at high temperatures, we deposited Pt on plated Au by vacuum evaporation. The thickness of Pt is approximately 1000Å.

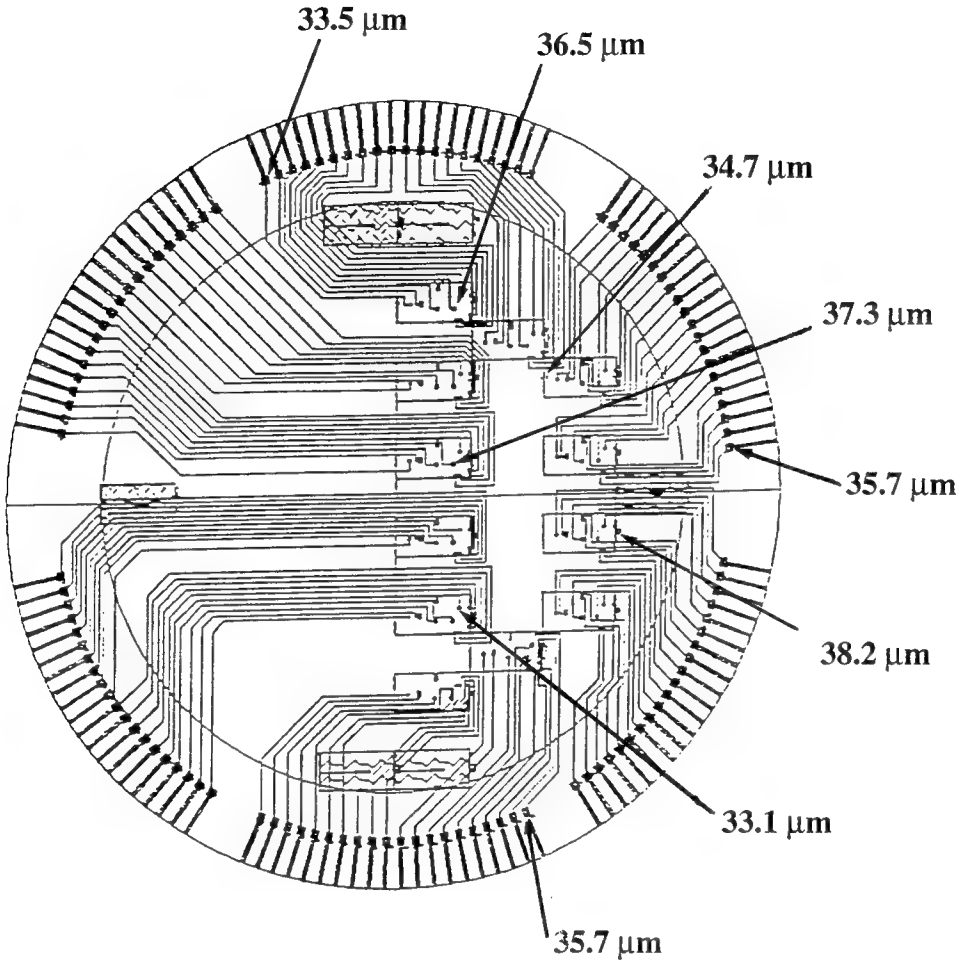
Etching Plating Medium and Cleaning
The final CIS fabrication process was to etch the plating medium Au/Ti after dissolving photoresist.

A completed CIS wafer is shown in Figure 34.

2.2.4 CIS Fabrication with Kapton Polyimide Substrate

Because of challenges in contacting the CIS built on glass substrate, we redirected our effort to concentrate on Kapton polyimide per Rome Lab's suggestion. The fabrication process is essentially identical to using glass substrate. However, because of mechanical and thermal stress, the thin film had a tendency to curl-up during metallization and photolithographic processes. To alleviate this we used a thicker polyimide (5 mils) and fabricated a fixture to keep the film flat during metallization and gold plating. In addition, we metallized both sides of wafer to equalize the mechanical stress. The thicker Kapton polyimide held up much better than the thin substrate.

For liquid polyimide coating on Kapton, we did not use adhesion promoter since excellent bonding between liquid polyimide and kapton polyimide is well known. The CIS fabrication process was successful until the last photolithography at which time we lost two wafers because of curling-up after plating medium metallization. We also lost two more wafers during the last cleaning step when the plated Au bumps pealed off while removing the photoresist.



Average: 35.6 ± 1.8 µm

Figure 33. Contact Bump Thickness Mapping

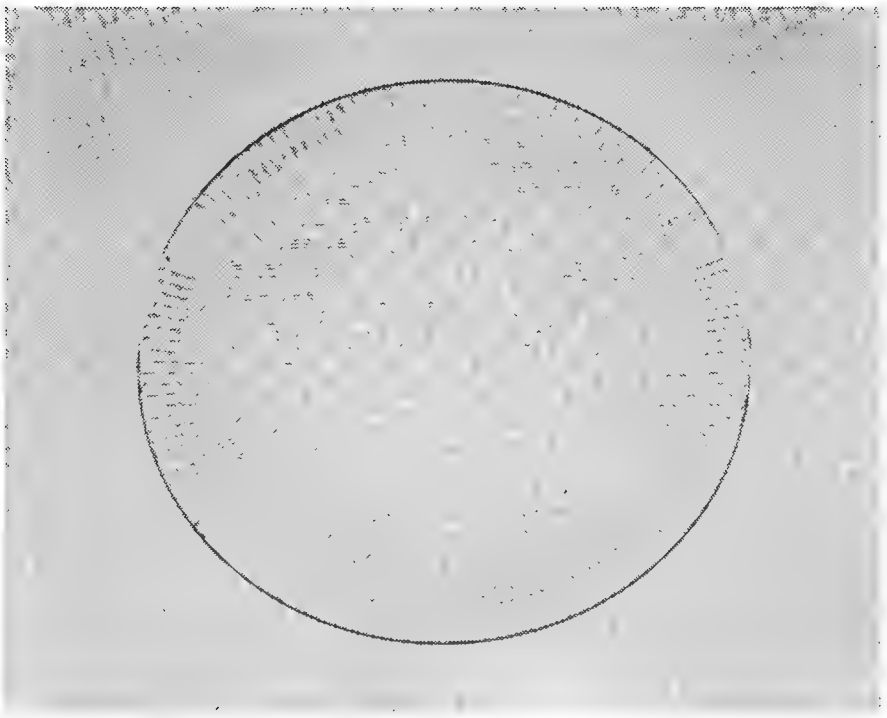


Figure 34. Completed CIS Glass Wafer

Apparently, the adhesion between Kapton polyimide and Ti was poor because the Kapton substrate could have been contaminated.

Another disadvantage of using Kapton polyimide as a substrate is that the film tends to shrink and expand due to heating and moisture absorption during the various processes. For a thick Kapton polyimide, a major factor is film shrinkage while curing the liquid polyimide. The largest misalignment was observed at both ends (large contact pads between CIS and ceramic plate). Measurement of the worst case of misalignment was valued as 80-90μm at maximum (a distance from a center of 4" wafer is 44 mm) as illustrated in Figure 35. Since the outer contact pads are 800mm square, 80-90μm (~10%) misalignment had no affect at all. For SEC and TCV contact, the farthest TCV is at 28 mm from the center and the misalignment is approximately 50μm. However, because of over plating of the contact pad (about 50 μm), misalignment of 50μm does not affect the contact.

2.2.5 Contact Bump Formation by Fuzzy Ball on Glass Substrate

For better contact between the CIS bump and dc contact pads on GaAs wafer, we implemented fuzzy ball bumps. This was developed for a button contact at TRW. The fuzzy ball is made of Au plated with BeCu. The balls were attached by conductive epoxy that withstands temperatures up to 175°C. Although these fuzzy balls are attached manually, and the heights are not well controlled in comparison to plating, excellent contact was made because of its remarkably springy property. Figure 36 shows one of the fuzzy balls attached to the contact bump.

2.3 MMIC PACKAGING AND DC/RF CHARACTERIZATION

2.3.1 MMIC Packaging

Distributed amplifier (DA) for constant stress life test of packaged MMIC was assembled by TRW's well established packaging procedure. Figure 37 shows a ceramic package

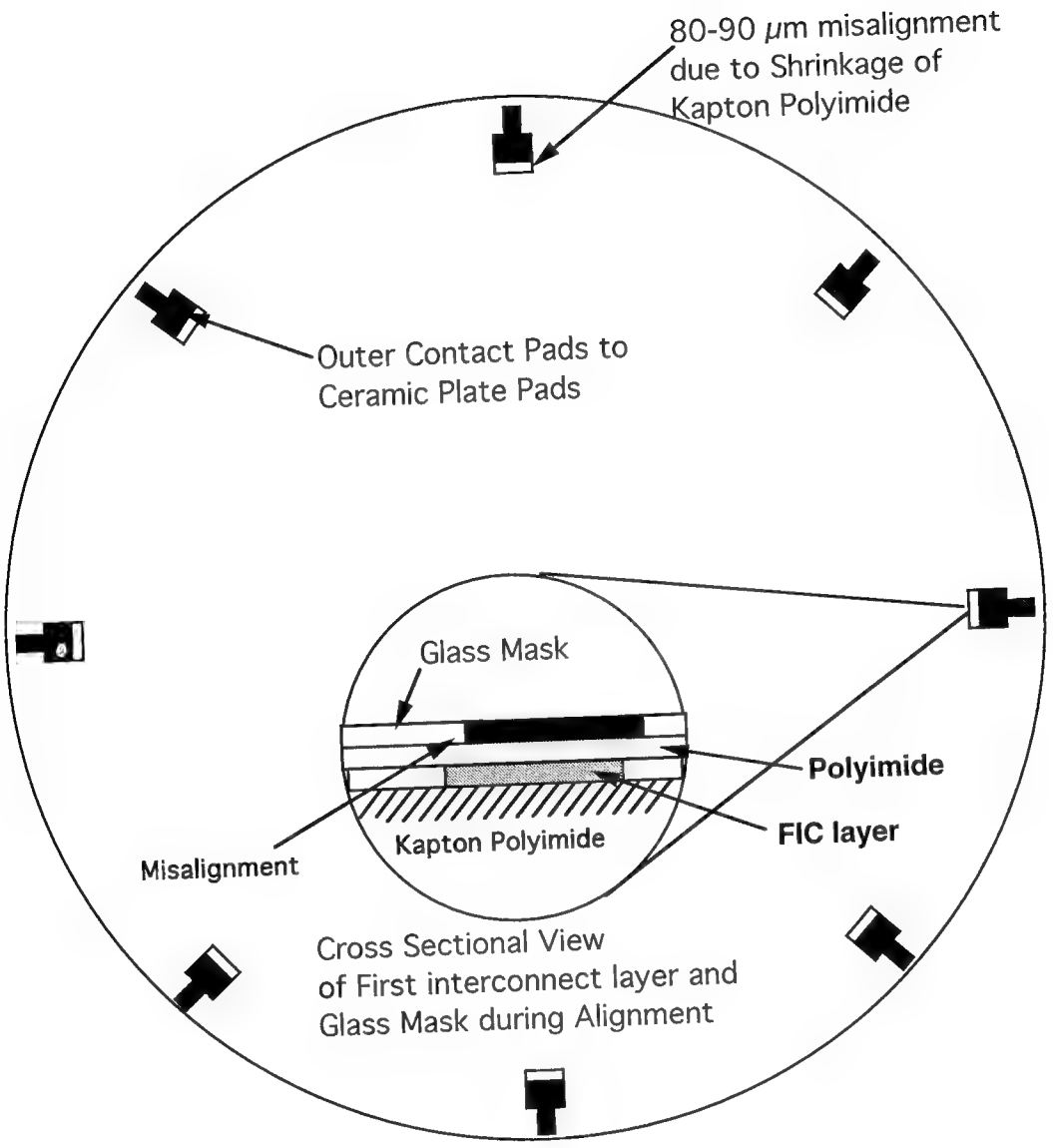


Figure 35. Illustration of a Shrinking of Kapton Polyimide During Curing Process

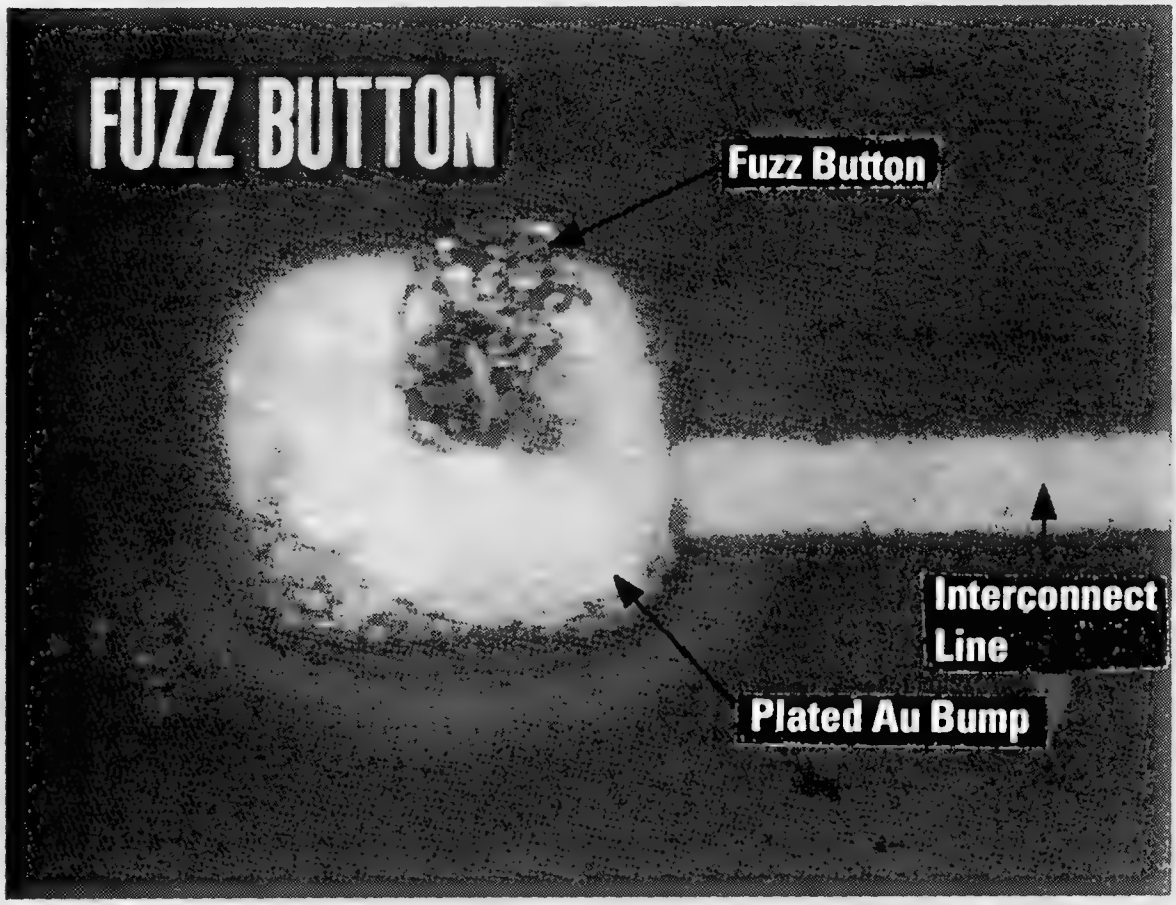


Figure 36. Photograph of the Fuzz Button Contact

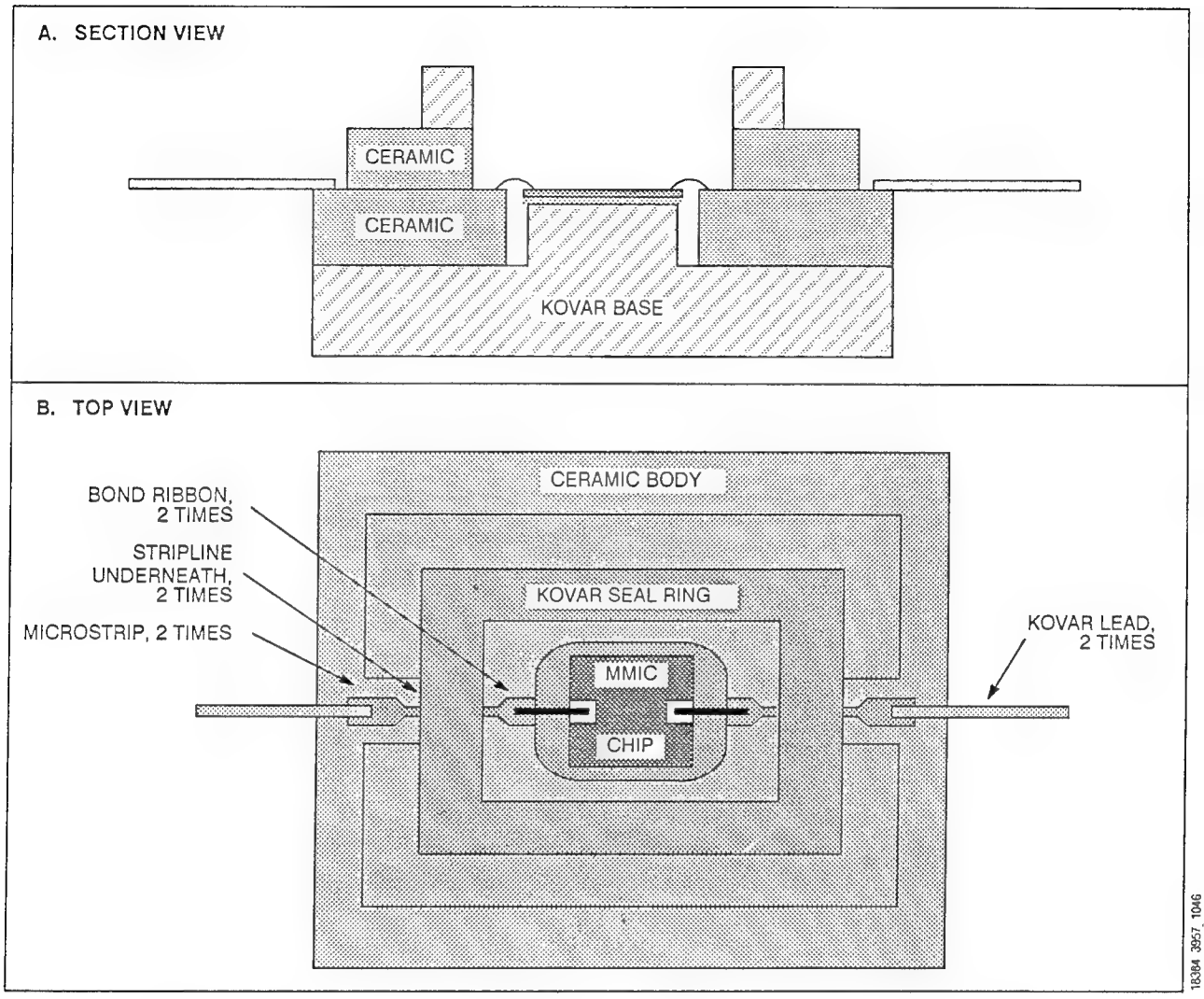


Figure 37. Conceptual Drawing of DA SEC Ceramic Package

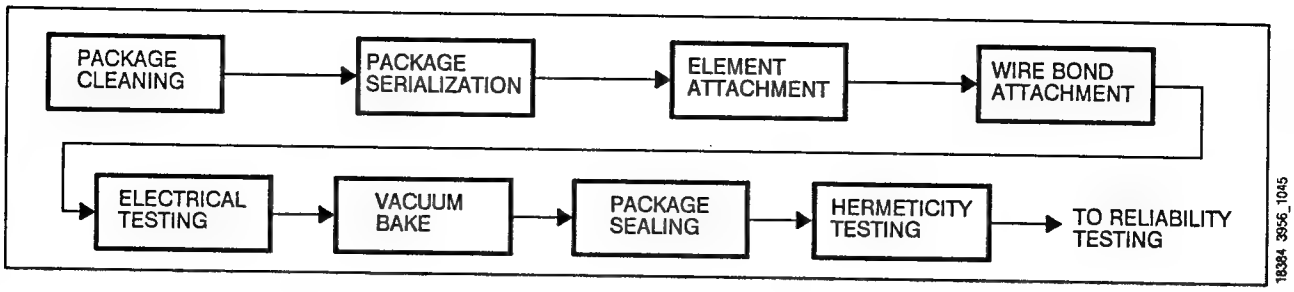


Figure 38. Basic Assembly Flow for Packaged DA SEC

that was used for wafer qualification of flight production. A flow diagram of MMIC assembly is shown in Figure 38. Package cleaning was performed by conventional solvent cleaning followed by serialization. DAs were mounted using AuSn eutectic. Gold wires and ribbons are attached to interconnect the MMIC die and the package microstrip lines. Using "soft-touch" thermosonic wedge bonders, excellent bonding strength is achieved without damaging the brittle GaAs substrate. Per Rome Lab's permission, the package was left unsealed because these DAs are passivated and glassivated, thus hermetic sealing for the life test was not necessary.

2.3.2 DC/RF Characterization

The packaged DAs were evaluated using RF test fixture as shown in Figure 39. This fixture was designed and fabricated by TRW's flight production program. Note: because dc bias pads and RF pads were the same (see Figure 11), cascade probing was not possible due to wire bonding on the pads. A HP 8510C was used to measure s-parameters. Figure 40 shows an example of the s-parameters, and Figure 41 shows the summary of the test results. The linear gain was measured at center frequency of 4.5 GHz. The variation between devices is 4.2-4.5 dB, which is excellent compared to previous flight production lots. The gain variation range of the flight production lots was 3.5-4.5 dB.

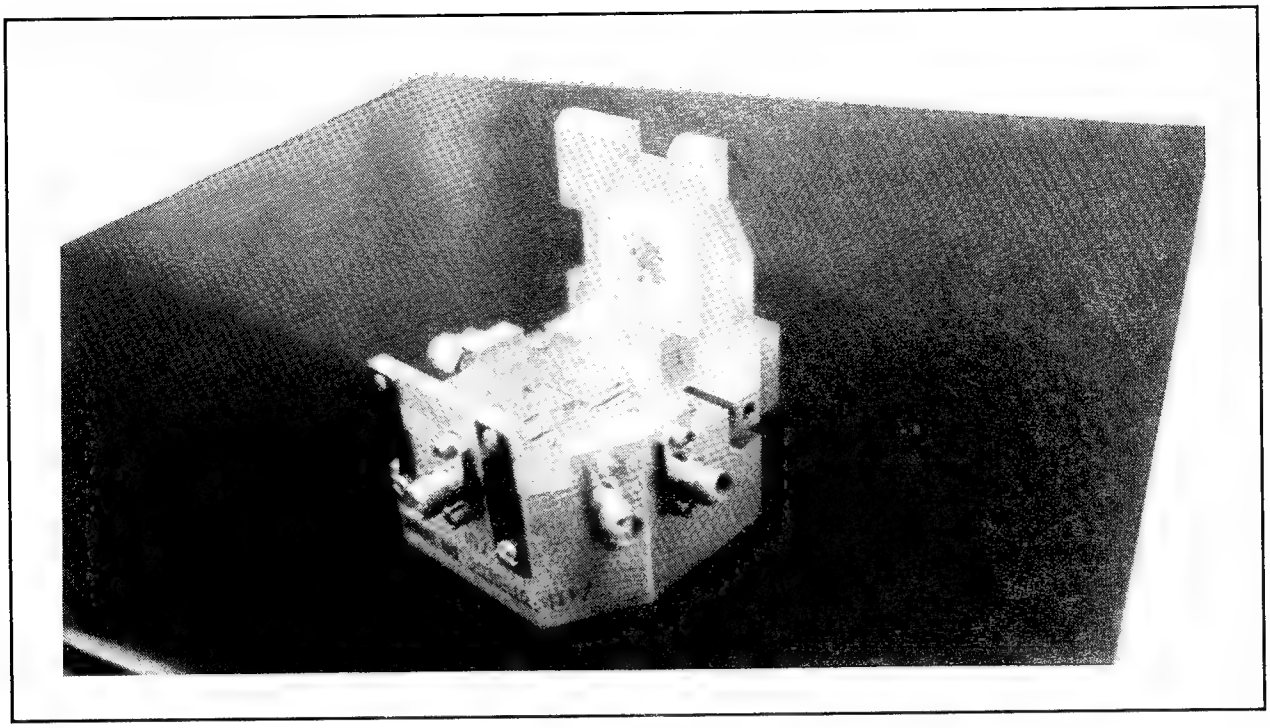


Figure 39. MMIC dc/RF Test Fixture

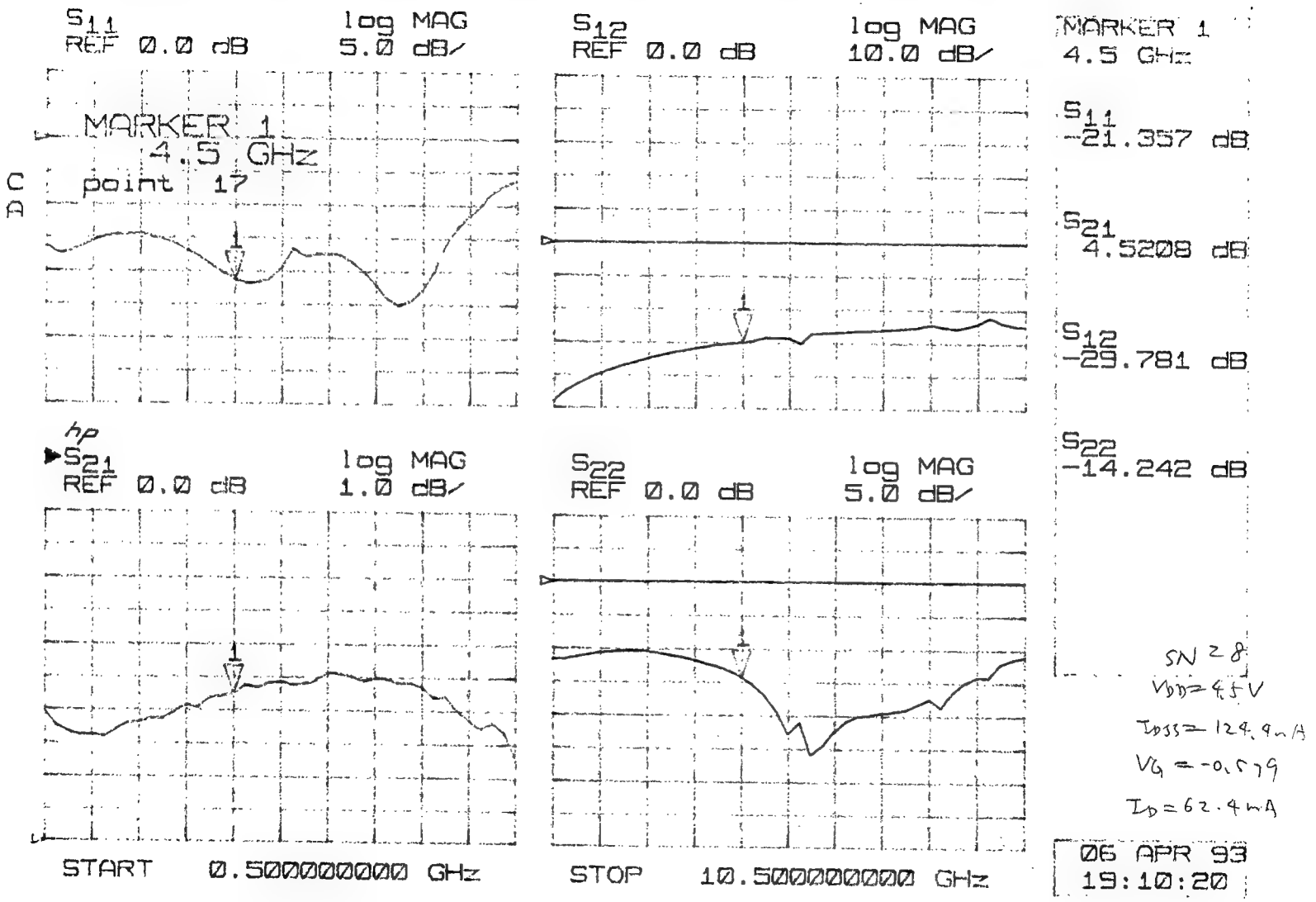


Figure 40. S-Parameters of OWR-4, Packaged SEC

OWR-4

Vdd=4.5V

	S/N	Idss (mA)	Vg at 0.5 Idss	S21 (dB)	S11(dB)	S22 (dB)
1	20	148.40	-0.73	4.26	-25.34	-14.27
2	22	111.71	-0.57	4.40	-25.30	-14.91
3	23	133.68	-0.66	4.26	-20.52	-13.08
4	24	152.61	-0.77	4.16	-22.46	-13.46
5	25	139.16	-0.68	4.21	-20.17	-14.08
6	26	151.73	-0.77	4.07	-23.05	-13.67
7	27	143.89	-0.69	4.45	-22.45	-14.97
8	28	124.40	-0.58	4.52	-21.36	-14.24
9	29	128.80	-0.61	4.57	-27.58	-16.00
10	30	106.15	-0.49	4.31	-13.79	-12.27
11	31	123.60	-0.58	4.52	-13.78	-12.27
12	32	110.37	-0.51	4.53	-13.77	-11.42
13	34	138.10	-0.68	4.49	-15.67	-13.06
14	35	145.29	-0.68	4.42	-14.80	-12.35
15	36	118.14	-0.56	4.37	-14.52	-12.39
16	41	134.70	-0.65	4.45	-17.35	-14.77
17	43	119.90	-0.55	4.68	-15.22	-13.45
18	44	142.10	-0.69	4.40	-15.06	-12.70
19	45	119.70	-0.55	4.61	-21.81	-17.81
20	46	150.60	-0.73	4.58	-22.49	-15.44
21	47	152.70	-0.77	4.17	-15.42	-12.94
22	48	148.70	-0.74	4.08	-14.34	-11.38
23	49	130.40	-0.63	4.29	-15.11	-13.14
24	50	128.17	-0.61	4.36	-13.27	-12.91
	AVE	133.46	-0.64	4.38	-18.53	-13.62

Figure 41. Summary of DC/RF Testing Results of Packaged SECs

2.4 LIFE TEST FIXTURE DESIGN, FABRICATION, AND ASSEMBLY

2.4.1 Fixture Design

The life test fixture was designed to perform wafer level high-temperature life test. The key requirements are: 1) able to operate at above 200°C ambient, 2) able to apply enough pressure evenly to the thinned 3" GaAs wafer without breaking it, 3) able to realign the contact pad of CIS and GaAs without disassembling the fixture.

To satisfy the first requirement, a ceramic interconnect plate was selected for the bias line connection between GaAs wafer and life test fixture bias connection. For meeting the second require-ments we designed a spring loaded plate for a GaAs wafer pedestal; the cover plate was also spring-loaded to prevent wafer breakage due to excess forces. To meet the third requirement, we designed a movable pedestal so that realignment can be done after the life test fixture assembly. Drawings for the life test fixture is attached in Appendix B.

2.4.2 Fixture Fabrication

The life test fixture was fabricated in TRW's machine shop. Main body was stainless steel and the wafer holding pedestal and CIS holder (top plate) were gold plated brass for better thermal conduction. Vacuum suction holes were made for both pedestal and top plate to hold GaAs wafer and CIS wafer, so that realignment can be done after assembly of the fixture. The wafer pedestal was designed to move approximately 2-3 mm x-y direction and rotational freedom for realignment by handles attached to both sides of the pedestal. Three see-through holes were also made to view the alignment marks on both the CIS and GaAs wafer.

The ceramic interconnect plate and connector plate to the high temperature oven were fabricated by DELTA-V Electronics in Campbell, CA. The interconnect lines were metallized (W/Ni/Au) on ceramic and heat treated to ensure the adhesion and stability during the high-temperature life test. However, because of the structure of the interconnect plate (thermal stress being concentrated at the thinnest part of the plate), the manufacturer had difficulty in this heat

treatment. The first ceramic plate was shattered during the cool down cycle. With a modified cool down process, it was able to complete one plate. The manufacture also fabricated connectors that goes from the end of flexible tape cable to the connector on high-temperature oven.

Figures 42 and 43 show an assembled life test fixture and exploded view of the fixture. Figure 44 shows that the life test fixture is in the high-temperature oven.

2.5 INTEGRATION AND TEST

2.5.1 Verification of the Integrity of Liquid Polyimide

Using organic materials for high-temperature life test may cause undesirable chemicals that might damage the electrical performance of a GaAs device. We conducted a verification test on Kapton polyimide and liquid polyimide at elevated temperatures. The stabake experiments were done on one of the wafers from the OWR-1 lot. The test wafer was split into two: one for a high temperature control sample, and the other for the CIS integrity test. Both wafers were loaded into the high-temperature oven. The processed CIS (with polyimide) wafer was in direct contact with the GaAs wafer during the stabake. The stabake of both wafers was done at 240°C for 48 hours in the high-temperature oven a with constant flow of nitrogen (identical condition as planned on wafer life test). We measured electrical parameters before and after the stabake. Figure 45 summarizes the stabake results. The C1,2,3... and R1,2,3.. designate the column and row of GaAs wafer. R1 through R6 are the one half wafer exposed to polyimide during the stabake, and R7 through R12 are the other half wafer as a high-temperature control sample. As shown in Figure 45 there is no difference in the ΔIdss and ΔGm between the presence and absence of polyimide. It is clear that the

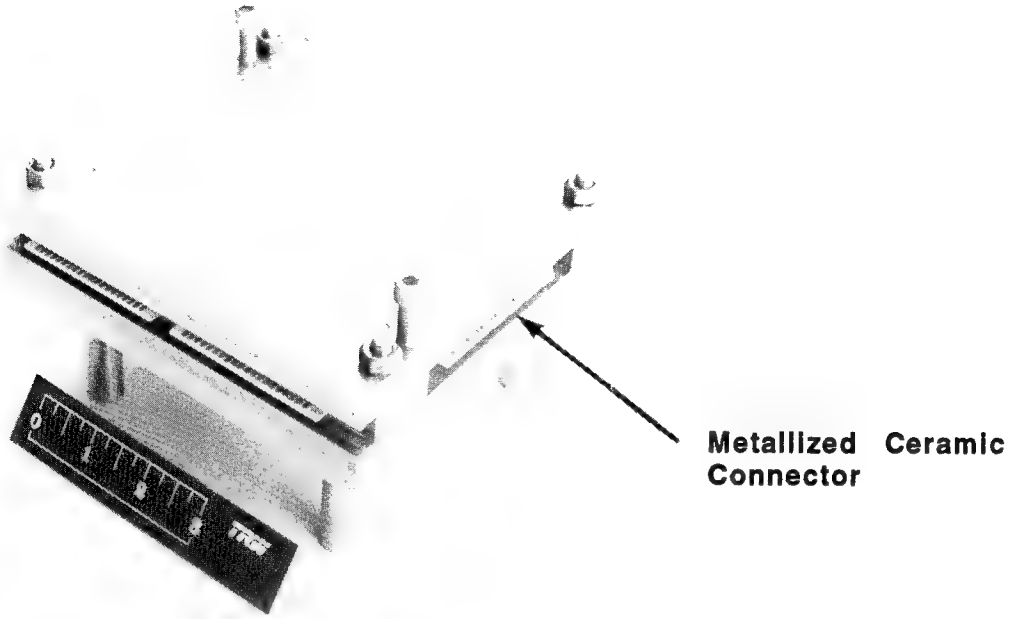


Figure 42. Assembled On-Wafer Life Test Fixture

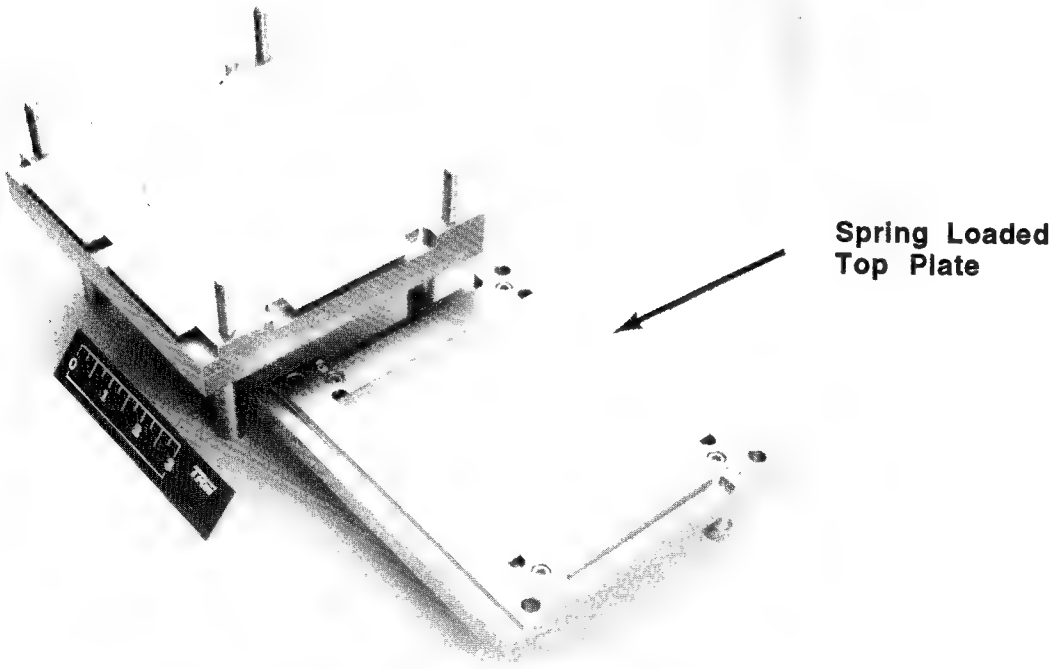


Figure 43. Open View of On-Wafer Life Test Fixture

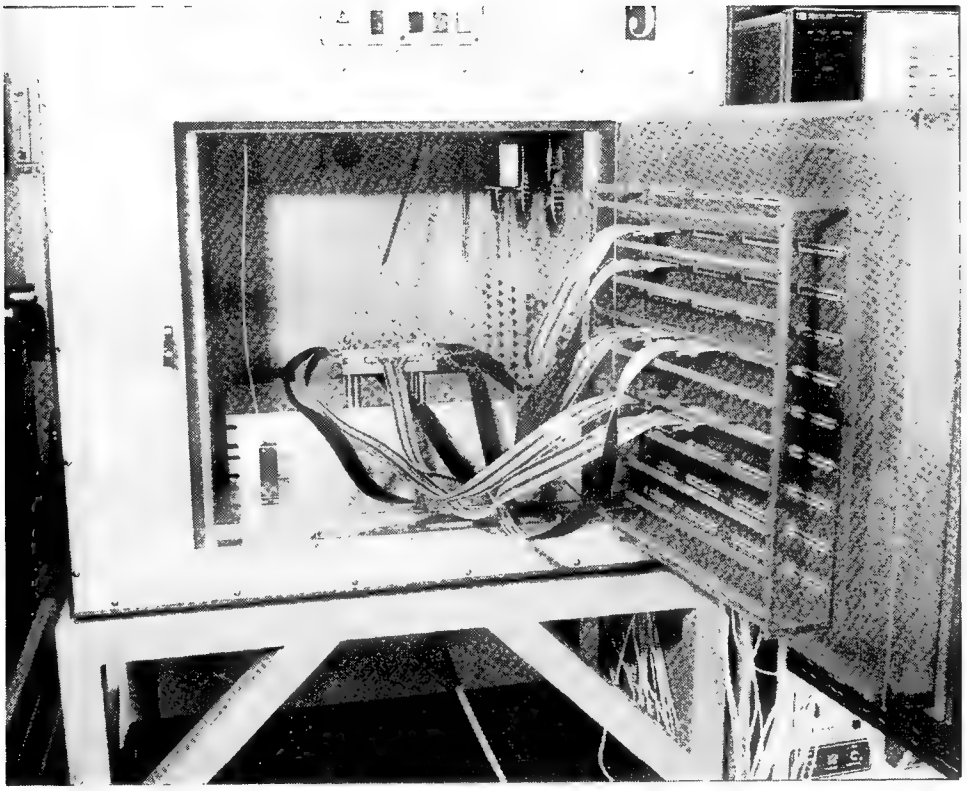


Figure 44. On-Wafer Life Test Fixture Installed in High-Temperature Oven

Idss change after stabaked at 240°C for 48 hours												
IN THE PRESENCE OF POLYIMIDE												
	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	AVE	
R1		0.00%	-27.80%	-25.71%	-17.78%	-16.81%	-13.62%	-17.39%	-22.91%	-31.34%	-19.26%	
R2		-19.14%	-20.04%	-28.61%	-15.87%	-19.34%	-10.91%	-16.63%	-18.27%	-24.60%	-19.27%	
R3		-21.99%	-16.22%	-11.38%	-7.89%	-	-9.77%	-13.18%	-13.65%	-20.92%	-14.38%	
R4		-19.41%	-11.88%	-8.61%	-9.48%	-	-10.01%	-8.45%	-10.16%	-16.66%	-11.83%	
R5	-23.23%	-16.75%	-	-8.62%	-8.78%	-	-10.65%	-5.53%	-	-17.79%	-9.73%	
R6	-23.37%	-10.27%	-8.53%	-5.79%	-7.58%	-6.05%	-8.64%	-9.93%	-9.98%	-19.08%	-8.59%	
AVE	-23.30%	-14.59%	-16.89%	-14.79%	-11.23%	-10.55%	-10.60%	-11.85%	-14.99%	-21.73%	AVE	-15.05%
											-13.84%	
IN THE ABSENCE OF POLYIMIDE												
	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	AVE	
R7	-24.80%	-15.40%	-11.27%	-15.06%	-10.54%	-8.36%	-15.46%	-9.07%	-9.94%	-13.16%	-10.83%	
R8	-22.40%	-14.20%	-10.61%	-7.40%	-8.25%	-7.26%	-8.01%	-6.82%	-9.37%	-12.01%	-8.39%	
R9		-21.60%	-13.71%	-10.70%	-8.14%	-8.23%	-12.29%	-13.49%	-10.85%	-12.65%	-12.41%	
R10		-20.50%	-14.53%	-12.13%	-10.11%	-12.40%	-8.63%	-7.89%	-13.50%	-15.20%	-12.77%	
R11		-34.90%	-21.37%	-23.47%	-17.00%		-11.50%	-14.35%	-15.42%	-26.06%	-20.51%	
R12		-	-27.72%	-26.70%	-21.90%		-12.98%	-19.00%	-24.80%	-24.41%	-22.50%	
AVE	-23.60%	-21.32%	-16.54%	-15.91%	-12.66%	-9.06%	-11.48%	-11.77%	-13.98%	-17.25%	AVE	-15.36%
											-14.57%	

C1, C2.....: Column
R1,R2.....: Row

Figure 45. Verification of the Integrity of Polyimide at High Temperature

decrease of Idss is strictly due to a thermal degradation, not due to polyimide. This test concluded that polyimide can be used as CIS material for high-temperature life testing.

2.5.2 Measurement of Resistance of Interconnect Lines of the CIS

We measured the resistance of the interconnect lines and contact pads of the CIS. For both glass and Kapton polyimide substrate, the resistance is minimal; the values were 0.1-0.2 Ω.

2.5.3 Measurements of Contact Resistance Between the CIS and GaAs Wafer Contact Pads

The contact resistance measurements were performed after assembling the GaAs wafer and the CIS in the life test fixture. Figure 46 summarizes the contact resistance of all gate, top metal TCVs.

2.6 COST ANALYSIS OF PACKAGED AND ON-WAFER LIFE TESTING

We conducted a cost analysis to compare the cost between packaged, and on-wafer life testing of the SECs and TCVs. Two cases were considered for this analysis: (1) Wafer completed backside process, (2) Wafer processed to top metal (Note: ground via cannot be used as ground contact for SECs and TCVs).

Case 1. Figure 47 shows the labor hour estimation for the packaged and on-wafer life testing. Assuming that a total of 10 SECs and 50 TCVs will be life tested, labor hours for chip separation and picking are based on one wafer. The labor hour estimation is based on historical data. Device packaging includes cleaning of AuSn preform and 16 pin DIP, serialization, die mounting, wire bonding, and visual inspection. DC and RF testing for the packaged SECs and TCVs require approximately 65% more time than on-wafer testing because loading and unloading the 16 pin DIP carrier will take time for each SEC and TCV. On-wafer life test will save over 200 hours per wafer.

Case 2. Figure 48 shows the labor hour estimation for the packaged and on-wafer (wafer processed to top metal) life testing. We also assumed that a total of 10 SECs and 50 TCVs will be life tested. However, in this case, labor hours for backside process are included in the packaged SECs and TCVs for comparison between the packaged and on-wafer life test. On-wafer life test will save over 300 hours per wafer.

Contact ID No.	Reticle No.	SEC/TCV ID.	Contact R (Ω)
A5	A1-5	Air bridge-hot	No Contact
A6	A1-6	TM-hot	No Contact
A7	A1-7	Gate metal-hot	2.5Ω
A15	A2-5	Air bridge-hot	2.6Ω
A16	A2-6	TM-hot	2.5Ω
B5	B1-5	Air bridge-hot	No Contact
B15	B2-5	Air bridge-hot	2.5Ω
C5	C1-5	Air bridge-hot	No Contact
D5	D1-5	Air bridge-hot	2.6Ω
D6	D1-6	TM-hot	2.5Ω
D7	D1-7	Gate metal-hot	2.6Ω
D15	D2-5	Air bridge-hot	2.6Ω
D16	D2-6	TM-hot	2.5Ω
D17	D2-7	Gate metal-hot	No Contact
E5	E1-5	Air bridge-hot	2.7Ω
E6	E1-6	TM-hot	2.7Ω
E7	E1-7	Gate metal-hot	2.6Ω
F5	F1-5	Air bridge-hot	2.4Ω
F6	F1-6	TM-hot	2.5Ω
F7	F1-7	Gate metal-hot	2.5Ω
F15	F2-5	Air bridge-hot	2.6Ω
F16	F2-6	TM-hot	2.5Ω
F17	F2-7	Gate metal-hot	2.4Ω

Figure 46. Summary of Contact Resistance Measured on the CIS-GaAs Wafer

Labor Hours are based on One Wafer
Quantity of SECs 10
Quantity of TCVs 50

		Labor (Hours)		
Task Description	Quantity	Packaged	On-Wafer	Comments
Chip Separation/Pick	1 Wafer/ 60 chips	30	0	
Chip Packaging	60 chips	120	0	
Wafer Mouting	1 Wafer	0	10	
DC/RF Testing	10 Times	200	120	Packaged chips are on fixture On-wafer testing is automated
Burn-in	1 Time	35	35	
Lifetest	8 Cycles	84	84	
Management/Business		60	60	
Total Labor Hours		529	309	
Carrier/CIS		$400	$1,000	

Figure 47. Cost Analysis of Packaged and On-Wafer Life Testing

Labor Hours are based on One Wafer
Quantity of SECs 10
Quantity of TCVs 50

		Labor (Hours)		
Task Description	Quantity	Packaged	On-Wafer	Comments
Backside Process	1 Wafer	80		
Chip Separation/Pick	1 Wafer/ 60 chips	30	0	
Chip Packaging	60 chips	120	0	
Wafer Mounting	1 Wafer	0	10	
DC/RF Testing	10 Times	200	120	Packaged chips are on fixture On-wafer testing is automated
Burn-in	1 Time	35	35	
Lifetest	8 Cycles	84	84	
Management/Business		60	40	
Total Labor Hours		609	289	
Carrier/CIS		$400	$1,000	

Figure 48. Cost Analysis of Packaged and On-Wafer (at Top Metal) Life Testing

3. SUMMARY

We have developed a technique for on-wafer reliability testing using TRW's COIN technology [we renamed it as Compliant Interconnect Structure (CIS)] and proved this concept of on-wafer level life testing can be implemented to reduce cost and schedule of reliability testing of GaAs devices and/or MMICs. Accomplishment of this program can be summarized as follows:

- Designed and fabricated 0.5μm MESFET SECs, six different types of TCVs on 3" wafer
- Designed CIS and fabricated mask set
- Developed CIS process on glass substrate and Kapton polyimide
- Implemented fuzzy ball bump contact developed by TRW for on-wafer bump contact
- Demonstrated excellent contact between GaAs contact pads to dc bias cards.

4. RECOMMENDATION TO FUTURE STUDY

We demonstrated the feasibility of on-wafer reliability testing methodology in this program, however we have not performed life testing using the developed technique. Therefore, the obvious recommendation is to carry out the on-wafer life test. Furthermore, this technique can be implemented in the life test of discrete devices. The life tests of discrete MESFET, HEMT, or HBT are difficult due to an oscillation problem. However using this CIS technique, the matching circuits can be fabricated on the CIS right next to contact pads. More importantly, this CIS technique can be used for the bases of multilayer technology, i.e., packaging MMICs without using wires; and for power amplifiers, additional thermal dissipation can be allowed through multilayer thin film. The following subjects can be recommended for the future study:

- Complete the accelerated life tests using the CIS technique
- Implement this methodology for discrete device life testing
- Apply this technique to multilayer thin film (multichip module) for power amplifiers.

5. APPENDICES

APPENDIX A

PCM DATA for OWR-4

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4POB206068 STATION : 1
OPERATOR : 110488
TEMP : AMBIENT

LOG FILE : OWR4POB206068
PAR FILE : [APTPRG.PAR]OWRPOB
LIM FILE : [APTPRG.LIM]OWRPOB
COMMENTS : .5U MESFET @ POST OHM
OWR TEG-.5U MESFET @ POST OHMIC(R2 FIELDS)

DATE : 31-JUL-92
LOG DATE : 31-JUL-92
LOG TIME : 11:26:34
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION		UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOLIM	LOSPEC	HISPEC	HILIM	MIN	MAX	MEAN	STD DEV	COEF
RSMESA Rsh	@ I= 1mA	Ohms/sq.	6	0	0	0	0	6	140.0	160.0	240.0	240.0	179.7	189.6	183.9	4.0	
RCOCA Rc	@ I= 10mA	Ohms	6	0	0	0	0	6	10.0m	10.0m	300.0m	300.0m	73.9m	87.8m	81.7m	5.2m	
OCTLMA Rc	@ I= 1mA	Ohms-mm	6	0	0	0	0	6	10.0m	10.0m	300.0m	300.0m	166.3m	232.1m	200.8m	27.3m	1
OCTLMA Rsh	@ I= 1mA	Ohms/sq.	6	0	0	0	0	6	140.0	160.0	240.0	240.0	201.1	208.1	204.6	3.0	
OCTLMA R5	@ I= 1mA	Ohms	6	0	0	0	0	6	1.0	1.0	50.0	50.0	26.2	29.5	27.9	1.2	
OCTLMA R10	@ I= 1mA	Ohms	6	0	0	0	0	6	1.0	1.0	100.0	100.0	48.0	52.1	50.1	1.4	
OCTLMA R15	@ I= 1mA	Ohms	6	0	0	0	0	6	1.0	1.0	200.0	200.0	66.4	71.1	68.9	1.6	
HVFET-ISOC Ids	@ V= 3V	mA/mm	6	0	0	0	0	6	300.0	300.0	2.0k	2.0k	1.5k	1.6k	1.6k	34.2	
HVFET-ISOC Viso	@ I=20mA	Volts	6	0	0	0	0	6	5.0	5.0	20.0	20.0	9.4	10.2	9.7	290.2m	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4POB206067 STATION : 1
OPERATOR : 110488
TEMP : AMBIENT

LOG FILE : OWR4POB206067
PAR FILE : [APTPRG.PAR]OWRPOB
LIM FILE : [APTPRG.LIM]OWRPOB
COMMENTS : .5U MESFET @ POST OHM
OWR TEG-.5U MESFET @ POST OHMIC(R2 FIELDS)

DATE : 31-JUL-92
LOG DATE : 31-JUL-92
LOG TIME : 11:25:11
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION		UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOLIM	LOSPEC	HISPEC	HILIM	MIN	MAX	MEAN	STD DEV	COEF
RSMESA Rsh	@ I= 1mA	Ohms/sq.	6	0	0	0	0	6	140.0	160.0	240.0	240.0	184.2	191.8	187.3	3.1	
RCOCA Rc	@ I= 10mA	Ohms	6	0	0	0	0	6	10.0m	10.0m	300.0m	300.0m	55.2m	71.7m	63.5m	5.4m	
OCTLMA Rc	@ I= 1mA	Ohms-mm	6	0	0	0	0	6	10.0m	10.0m	300.0m	300.0m	224.7m	248.2m	234.3m	8.7m	
OCTLMA Rsh	@ I= 1mA	Ohms/sq.	6	0	0	0	0	6	140.0	160.0	240.0	240.0	200.0	206.5	203.2	2.6	
OCTLMA R5	@ I= 1mA	Ohms	6	0	0	0	0	6	1.0	1.0	50.0	50.0	28.7	29.7	29.1	455.3m	
OCTLMA R10	@ I= 1mA	Ohms	6	0	0	0	0	6	1.0	1.0	100.0	100.0	50.4	52.1	51.1	643.5m	
OCTLMA R15	@ I= 1mA	Ohms	6	0	0	0	0	6	1.0	1.0	200.0	200.0	68.7	71.0	69.8	848.3m	
HVFET-ISOC Ids	@ V= 3V	mA/mm	6	0	0	0	0	6	300.0	300.0	2.0k	2.0k	1.5k	1.5k	1.5k	11.1	
HVFET-ISOC Viso	@ I=20nA	Volts	6	0	0	0	0	6	5.0	5.0	20.0	20.0	10.6	10.9	10.7	118.8m	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4POB206066 STATION : 1
OPERATOR : 110488
TEMP : AMBIENT

LOG FILE : OWR4POB206066
PAR FILE : [APTPRG.PAR]OWRPOB
LIM FILE : [APTPRG.LIM]OWRPOB
COMMENTS : .5U MESFET @ POST OHM
OWR TEG-.5U MESFET @ POST OHMIC(R2 FIELDS)

DATE : 31-JUL-92
LOG DATE : 31-JUL-92
LOG TIME : 11:23:49
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION		UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOLIM	LOSPEC	HISPEC	HILIM	MIN	MAX	MEAN	STD DEV	COEF
RSMESA Rsh	@ I= 1mA	Ohms/sq.	6	0	0	0	0	6	140.0	160.0	240.0	240.0	181.3	191.3	185.7	3.8	
RCOCA Rc	@ I= 10mA	Ohms	6	0	0	0	0	6	10.0m	10.0m	300.0m	300.0m	65.4m	87.7m	76.4m	8.0m	1
OCTLMA Rc	@ I= 1mA	Ohms-mm	6	0	0	0	0	6	10.0m	10.0m	300.0m	300.0m	222.0m	258.8m	243.4m	14.1m	
OCTLMA Rsh	@ I= 1mA	Ohms/sq.	6	0	0	0	0	6	140.0	160.0	240.0	240.0	195.4	205.1	200.4	3.5	
OCTLMA R5	@ I= 1mA	Ohms	6	0	0	0	0	6	1.0	1.0	50.0	50.0	28.5	29.7	29.2	430.0m	
OCTLMA R10	@ I= 1mA	Ohms	6	0	0	0	0	6	1.0	1.0	100.0	100.0	50.4	51.7	51.0	594.6m	
OCTLMA R15	@ I= 1mA	Ohms	6	0	0	0	0	6	1.0	1.0	200.0	200.0	68.1	70.2	69.3	893.3m	
HVFET-ISOC Ids	@ V= 3V	mA/mm	6	0	0	0	0	6	300.0	300.0	2.0k	2.0k	1.4k	1.5k	1.5k	21.8	
HVFET-ISOC Viso	@ I=20nA	Volts	6	0	0	0	0	6	5.0	5.0	20.0	20.0	10.6	10.9	10.8	112.1m	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4POB206064 STATION : 1
OPERATOR : 110488
TEMP : AMBIENT

LOG FILE : OWR4POB206064
PAR FILE : [APTPRG.PAR]OWRPOB
LIM FILE : [APTPRG.LIM]OWRPOB
COMMENTS : .5U MESFET @ POST OHM
OWR TEG-.5U MESFET @ POST OHMIC(R2 FIELDS)

DATE : 31-JUL-92
LOG DATE : 31-JUL-92
LOG TIME : 11:22:27
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION		UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOLIM	LOSPEC	HISPEC	HILIM	MIN	MAX	MEAN	STD DEV	COEF
RSMESA Rsh	@ I= 1mA	Ohms/sq.	6	0	0	0	0	6	140.0	160.0	240.0	240.0	181.9	190.1	185.8	3.3	
RCOCA Rc	@ I= 10mA	Ohms	6	0	0	0	0	6	10.0m	10.0m	300.0m	300.0m	55.6m	74.9m	65.1m	8.6m	1
OCTLMA Rc	@ I= 1mA	Ohms-mm	6	0	0	0	0	6	10.0m	10.0m	300.0m	300.0m	230.1m	257.0m	239.5m	9.3m	
OCTLMA Rsh	@ I= 1mA	Ohms/sq.	6	0	0	0	0	6	140.0	160.0	240.0	240.0	197.0	204.5	200.6	3.3	
OCTLMA R5	@ I= 1mA	Ohms	6	0	0	0	0	6	1.0	1.0	50.0	50.0	28.7	30.2	29.0	583.7m	
OCTLMA R10	@ I= 1mA	Ohms	6	0	0	0	0	6	1.0	1.0	100.0	100.0	50.0	52.3	50.9	820.5m	
OCTLMA R15	@ I= 1mA	Ohms	6	0	0	0	0	6	1.0	1.0	200.0	200.0	68.1	71.1	69.2	1.2	
HVFET-ISOC Ids	@ V= 3V	mA/mm	6	0	0	0	0	6	300.0	300.0	2.0k	2.0k	1.4k	1.5k	1.5k	31.8	
HVFET-ISOC Viso	@ I=20nA	Volts	6	0	0	0	0	6	5.0	5.0	20.0	20.0	10.7	10.9	10.8	103.5m	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4POB206063 STATION : 1
OPERATOR : 110488
TEMP : AMBIENT

LOG FILE : OWR4POB206063
PAR FILE : [APTPRG.PAR]OWRPOB
LIM FILE : [APTPRG.LIM]OWRPOB
COMMENTS : .5U MESFET @ POST OHM
OWR TEG-.5U MESFET @ POST OHMIC(R2 FIELDS)

DATE : 31-JUL-92
LOG DATE : 31-JUL-92
LOG TIME : 11:21:06
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION		UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOLIM	LOSPEC	HISPEC	HILIM	MIN	MAX	MEAN	STD DEV	COEF
RSMESA Rsh	@ I= 1mA	Ohms/sq.	6	0	0	0	0	6	140.0	160.0	240.0	240.0	188.0	197.7	191.9	3.8	
RCOCA Rc	@ I= 10mA	Ohms	6	0	0	0	0	6	10.0m	10.0m	300.0m	300.0m	23.8m	36.7m	28.1m	5.2m	1
OCTLMA Rc	@ I= 1mA	Ohms-mm	6	0	0	0	0	6	10.0m	10.0m	300.0m	300.0m	197.3m	257.9m	224.3m	23.0m	1
OCTLMA Rsh	@ I= 1mA	Ohms/sq.	6	0	0	0	0	6	140.0	160.0	240.0	240.0	203.4	212.7	207.6	4.2	
OCTLMA R5	@ I= 1mA	Ohms	6	0	0	0	0	6	1.0	1.0	50.0	50.0	28.5	30.1	29.2	705.9m	
OCTLMA R10	@ I= 1mA	Ohms	6	0	0	0	0	6	1.0	1.0	100.0	100.0	50.6	52.9	51.7	829.0m	
OCTLMA R15	@ I= 1mA	Ohms	6	0	0	0	0	6	1.0	1.0	200.0	200.0	69.5	72.1	70.7	1.0	
HVFET-ISOC Ids	@ V= 3V	mA/mm	6	0	0	0	0	6	300.0	300.0	2.0k	2.0k	1.4k	1.5k	1.5k	12.2	
HVFET-ISOC Viso	@ I=20nA	Volts	6	0	0	0	0	6	5.0	5.0	20.0	20.0	10.6	10.9	10.7	104.9m	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4POB206062 STATION : 1
OPERATOR : 110488
TEMP : AMBIENT

LOG FILE : OWR4POB206062
PAR FILE : [APTPRG.PAR]OWRPOB
LIM FILE : [APTPRG.LIM]OWRPOB
COMMENTS : .5U MESFET @ POST OHM
OWR TEG-.5U MESFET @ POST OHMIC(R2 FIELDS)

DATE : 31-JUL-92
LOG DATE : 31-JUL-92
LOG TIME : 11:19:08
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION		UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOLIM	LOSPEC	HISPEC	HILIM	MIN	MAX	MEAN	STD DEV	COEF
RSMESA Rsh	@ I= 1mA	Ohms/sq.	6	0	0	0	0	6	140.0	160.0	240.0	240.0	193.9	201.1	197.0	3.0	
RCOCA Rc	@ I= 10mA	Ohms	6	0	0	0	0	6	10.0m	10.0m	300.0m	300.0m	59.3m	72.0m	65.8m	5.3m	
OCTLMA Rc	@ I= 1mA	Ohms-mm	6	0	0	0	0	6	10.0m	10.0m	300.0m	300.0m	236.2m	270.5m	258.2m	12.2m	
OCTLMA Rsh	@ I= 1mA	Ohms/sq.	6	0	0	0	0	6	140.0	160.0	240.0	240.0	200.5	210.4	204.8	3.6	
OCTLMA R5	@ I= 1mA	Ohms	6	0	0	0	0	6	1.0	1.0	50.0	50.0	29.9	30.8	30.3	341.9m	
OCTLMA R10	@ I= 1mA	Ohms	6	0	0	0	0	6	1.0	1.0	100.0	100.0	51.8	53.0	52.3	476.4m	
OCTLMA R15	@ I= 1mA	Ohms	6	0	0	0	0	6	1.0	1.0	200.0	200.0	70.1	72.1	71.2	831.5m	
HVFET-ISOC Ids	@ V= 3V	mA/mm	6	0	0	0	0	6	300.0	300.0	2.0k	2.0k	1.4k	1.4k	1.4k	25.2	
HVFET ISOC Viso	@ I=20nA	Volts	6	0	0	0	0	6	5.0	5.0	20.0	20.0	10.8	11.0	10.9	60.1m	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4TRB206062 STATION : 1
OPERATOR : 78395
TEMP : AMBIENT

LOG FILE : OWR4TRB206062
PAR FILE : [APTPRG.PAR]OWRTRB.PAR
LIM FILE : [APTPRG.LIM]OWRTRB
COMMENTS : .5U MESFET @ TFR
OWR TEG-.5U MESFET @ TFR (R2 FIELDS)

DATE : 31-AUG-92
LOG DATE : 31-AUG-92
LOG TIME : 09:24:00
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION	UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOFCNT	LOSPEC	HISPEC	HIFCNT	MIN	MAX	MEAN	STD DEV	COEF
RSTFRA Rsh @ I=1mA	Ohms/sq.	6	0	0	0	0	6	60.0	85.0	115.0	200.0	101.5	103.0	102.1	521.4m	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4TRB206063 STATION : 1
OPERATOR : 78395
TEMP : AMBIENT

LOG FILE : OWR4TRB206063
PAR FILE : [APTPRG.PAR]OWRTRB.PAR
LIM FILE : [APTPRG.LIM]OWRTRB
COMMENTS : .5U MESFET @ TFR
OWR TEG-.5U MESFET @ TFR (R2 FIELDS)

DATE : 31-AUG-92
LOG DATE : 31-AUG-92
LOG TIME : 09:25:04
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION	UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOFCNT	LOSPEC	HISPEC	HIFCNT	MIN	MAX	MEAN	STD DEV	COEF
RSTFRA Rsh @ I=1mA	Ohms/sq.	6	0	0	0	0	6	60.0	85.0	115.0	200.0	101.8	102.5	102.2	266.6m	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4TRB206064 STATION : 1
OPERATOR : 78395
TEMP : AMBIENT

LOG FILE : OWR4TRB206064
PAR FILE : [APTPRG.PAR]OWRTRB.PAR
LIM FILE : [APTPRG.LIM]OWRTRB
COMMENTS : .5U MESFET @ TFR
OWR TEG-.5U MESFET @ TFR (R2 FIELDS)

DATE : 31-AUG-92
LOG DATE : 31-AUG-92
LOG TIME : 09:26:20
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION	UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOFCNT	LOSPEC	HISPEC	HIFCNT	MIN	MAX	MEAN	STD DEV	COEF
RSTFRA Rsh @ I=1mA	Ohms/sq.	6	0	0	0	0	6	60.0	85.0	115.0	200.0	104.7	106.0	105.2	521.4m	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4TRB206066 STATION : 1
OPERATOR : 78395
TEMP : AMBIENT

LOG FILE : OWR4TRB206066
PAR FILE : [APTPRG.PAR]OWRTRB.PAR
LIM FILE : [APTPRG.LIM]OWRTRB
COMMENTS : .5U MESFET @ TFR
OWR TEG-.5U MESFET @ TFR (R2 FIELDS)

DATE : 31-AUG-92
LOG DATE : 31-AUG-92
LOG TIME : 09:27:45
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION	UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOFCNT	LOSPEC	HISPEC	HIFCNT	MIN	MAX	MEAN	STD DEV	COEF
RSTFRA Rsh @ I=1mA	Ohms/sq.	6	0	0	0	0	6	60.0	85.0	115.0	200.0	85.6	86.2	85.8	271.0m	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4TRB206067 STATION : 1
OPERATOR : 78395
TEMP : AMBIENT

LOG FILE : OWR4TRB206067
PAR FILE : [APTPRG.PAR]OWRTRB.PAR
LIM FILE : [APTPRG.LIM]OWRTRB
COMMENTS : .5U MESFET @ TFR
OWR TEG-.5U MESFET @ TFR (R2 FIELDS)

DATE : 31-AUG-92
LOG DATE : 31-AUG-92
LOG TIME : 09:29:01
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION	UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOFCNT	LOSPEC	HISPEC	HIFCNT	MIN	MAX	MEAN	STD DEV	COEF
RSTFRA Rsh @ I=1mA	Ohms/sq.	6	0	0	0	0	6	60.0	85.0	115.0	200.0	102.0	102.7	102.3	276.7m	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4TRB206068 STATION : 1
OPERATOR : 78395
TEMP : AMBIENT

LOG FILE : OWR4TRB206068
PAR FILE : [APTPRG.PAR]OWRTRB.PAR
LIM FILE : [APTPRG.LIM]OWRTRB
COMMENTS : .5U MESFET @ TFR
OWR TEG-.5U MESFET @ TFR (R2 FIELDS)

DATE : 31-AUG-92
LOG DATE : 31-AUG-92
LOG TIME : 09:29:59
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION	UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOFCNT	LOSPEC	HISPEC	HIFCNT	MIN	MAX	MEAN	STD DEV	COEF
RSTFRA Rsh @ I=1mA	Ohms/sq.	6	0	0	0	0	6	60.0	85.0	115.0	200.0	101.2	102.2	101.6	395.3m	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4PGT206068 STATION : 1
OPERATOR : 78395
TEMP : AMBIENT

LOG FILE : OWR4PGT206068
PAR FILE : [APTPRG.PAR]OWRPGT.PAR
LIM FILE : [APTPRG.LIM]OWRFET
COMMENTS : MESFET @ POST GATE TOP
OWR TEG-.5U MES. FET TEST @ POST GATE(R1 FIELDS)

DATE : 10-AUG-92
LOG DATE : 10-AUG-92
LOG TIME : 15:13:54
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION	UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOLIM	LOSPEC	HISPEC	HILIM	MIN	MAX	MEAN	STD DEV	COEF
HVFET ISOC Idss @ V=3 Volts	mA/mm	6	0	0	0	0	6	170.0	170.0	290.0	290.0	212.2	269.6	244.6	20.0	
HVFET ISOC GM0 @ Vgs=0	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	144.9	154.0	149.9	3.0	
HVFET-ISOC GM50 @Vgs=50%Idss	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	123.9	133.2	128.7	3.0	
HVFET-ISOC VP @ Ids=2%Idss	Volts	5	1	0	0	0	6	-3.0	-2.3	-1.3	-1.0	-2.3	-1.8	-2.1	185.2m	
HVFET ISOC BVgx @ Ig=10uA	Volts	6	0	0	0	0	6	-15.0	-15.0	-6.0	-1.0	-13.9	-13.5	-13.6	210.7m	
HVFET ISOC n Ideality Factor		6	0	0	0	0	6	1.0	1.0	2.0	2.0	1.1	1.1	1.1	2.2m	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4PGT206067 STATION : 1
OPERATOR : 78395
TEMP : AMBIENT

LOG FILE : OWR4PGT206067
PAR FILE : [APTPRG.PAR]OWRPGT.PAR
LIM FILE : [APTPRG.LIM]OWRFET
COMMENTS : MESFET @ POST GATE TOP
OWR TEG-.5U MES. FET TEST @ POST GATE(R1 FIELDS)

DATE : 10-AUG-92
LOG DATE : 10-AUG-92
LOG TIME : 15:12:40
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION	UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOLIM	LOSPEC	HISPEC	HILIM	MIN	MAX	MEAN	STD DEV	COEF
HVFET-ISOC Idss @ V=3 Volts	mA/mm	6	0	0	0	0	6	170.0	170.0	290.0	290.0	197.3	227.8	210.6	13.0	
HVFET-ISOC GM0 @ Vgs=0	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	156.2	162.7	159.5	3.3	
HVFET-ISOC GM50 @Vgs=50%Idss	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	139.5	148.8	143.9	4.5	
HVFET-ISOC VP @ Ids=2%Idss	Volts	6	0	0	0	0	6	-3.0	-2.3	-1.3	-1.0	-1.8	-1.5	-1.6	127.4m	
HVFET-ISOC BVgx @ Ig=10uA	Volts	6	0	0	0	0	6	-15.0	-15.0	-6.0	-1.0	-13.9	-13.1	-13.6	333.3m	
HVFET-ISOC n Ideality Factor		6	0	0	0	0	6	1.0	1.0	2.0	2.0	1.1	1.1	1.1	2.1m	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4PGT206066 STATION : 1
OPERATOR : 78395
TEMP : AMBIENT

LOG FILE : OWR4PGT206066
PAR FILE : [APTPRG.PAR]OWRPGT.PAR
LIM FILE : [APTPRG.LIM]OWRFET
COMMENTS : MESFET @ POST GATE TOP
OWR TEG-.5U MES. FET TEST @ POST GATE(R1 FIELDS)

DATE : 10-AUG-92
LOG DATE : 10-AUG-92
LOG TIME : 15:11:14
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION	UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOLIM	LOSPEC	HISPEC	HILIM	MIN	MAX	MEAN	STD DEV	COEF
HVFET-ISOC Idss @ V=3 Volts	mA/mm	6	0	0	0	0	6	170.0	170.0	290.0	290.0	189.4	232.2	211.4	13.9	
HVFET ISOC GM0 @ Vgs=0	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	155.6	162.4	159.4	2.6	
HVFET ISOC GM50 @Vgs=50%Idss	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	138.8	148.2	144.6	3.7	
HVFET-ISOC VP @ Ids=2%Idss	Volts	6	0	0	0	0	6	-3.0	-2.3	-1.3	-1.0	-1.8	-1.5	-1.6	125.7m	
HVFET ISOC BVgx @ Ig=10uA	Volts	6	0	0	0	0	6	-15.0	-15.0	-6.0	-1.0	-14.3	-13.5	-13.6	333.3m	
HVFET-ISOC n Ideality Factor		6	0	0	0	0	6	1.0	1.0	2.0	2.0	1.1	1.1	1.1	4.6m	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4PGT206064 STATION : 1
OPERATOR : 78395
TEMP : AMBIENT

LOG FILE : OWR4PGT206064
PAR FILE : [APTPRG.PAR]OWRPGT.PAR
LIM FILE : [APTPRG.LIM]OWRFET
COMMENTS : MESFET @ POST GATE TOP
OWR TEG-.5U MES. FET TEST @ POST GATE(R1 FIELDS)

DATE : 10-AUG-92
LOG DATE : 10-AUG-92
LOG TIME : 15:09:52
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION	UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOLIM	LOSPEC	HISPEC	HILIM	MIN	MAX	MEAN	STD DEV	COEF
HVFET-ISOC Idss @ V=3 Volts	mA/mm	6	0	0	0	0	6	170.0	170.0	290.0	290.0	184.1	237.0	207.8	18.2	
HVFET ISOC GM0 @ Vgs=0	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	156.3	162.6	159.5	2.3	
HVFET-ISOC GM50 @Vgs=50%Idss	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	137.4	142.9	140.3	2.0	
HVFET ISOC VP @ Ids=2%Idss	Volts	6	0	0	0	0	6	-3.0	-2.3	-1.3	-1.0	-1.9	-1.5	-1.7	153.6m	
HVFET-ISOC BVgx @ Ig=10uA	Volts	6	0	0	0	0	6	-15.0	-15.0	-6.0	-1.0	-14.3	-13.9	-14.0	210.6m	
HVFET ISOC n Ideality Factor		6	0	0	0	0	6	1.0	1.0	2.0	2.0	1.1	1.1	1.1	8.6m	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4PGT206063 STATION : 1
OPERATOR : 78395
TEMP : AMBIENT

LOG FILE : OWR4PGT206063
PAR FILE : [APTPRG.PAR]OWRPGT.PAR
LIM FILE : [APTPRG.LIM]OWRFET
COMMENTS : MESFET @ POST GATE TOP
OWR TEG-.5U MES. FET TEST @ POST GATE(R1 FIELDS)

DATE : 10-AUG-92
LOG DATE : 10-AUG-92
LOG TIME : 15:08:37
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION	UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOLIM	LOSPEC	HISPEC	HILIM	MIN	MAX	MEAN	STD DEV	COEF
HVFET ISOC Idss @ V=3 Volts	mA/mm	6	0	0	0	0	6	170.0	170.0	290.0	290.0	213.8	258.0	238.2	16.7	
HVFET ISOC GM0 @ Vgs=0	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	152.5	162.6	157.7	4.5	
HVFET-ISOC GM50 @Vgs=50%Idss	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	140.8	153.6	146.9	5.8	
HVFET ISOC VP @ Ids=2%Idss	Volts	6	0	0	0	0	6	-3.0	2.3	1.3	-1.0	-2.0	-1.6	-1.8	164.5m	
HVFET ISOC BVgx @ Ig=10uA	Volts	6	0	0	0	0	6	-15.0	15.0	-6.0	-1.0	13.9	13.1	-13.5	307.3m	
HVFET ISOC n Ideality Factor		6	0	0	0	0	6	1.0	1.0	2.0	2.0	1.1	1.1	1.1	5.0m	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4PGT206062 STATION : 1
OPERATOR : 78395
TEMP : AMBIENT

LOG FILE : OWR4PGT206062
PAR FILE : [APTPRG.PAR]OWRPGT.PAR
LIM FILE : [APTPRG.LIM]OWRFET
COMMENTS : MESFET @ POST GATE TOP
OWR TEG-.5U MES. FET TEST @ POST GATE(R1 FIELDS)

DATE : 10-AUG-92
LOG DATE : 10-AUG-92
LOG TIME : 15:07:01
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION	UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOLIM	LOSPEC	HISPEC	HILIM	MIN	MAX	MEAN	STD DEV	COEF
HVFET-ISOC Idss @ V=3 Volts	mA/mm	5	0	0	0	1	6	170.0	170.0	290.0	290.0	214.6	230.2	222.2	7.1	
HVFET-ISOC GM0 @ Vgs=0	mS/mm	5	0	0	0	1	6	90.0	120.0	300.0	300.0	160.3	164.4	162.5	1.7	
HVFET-ISOC GM50 @Vgs=50%Idss	mS/mm	5	0	0	0	1	6	90.0	120.0	300.0	300.0	142.8	147.7	146.2	2.1	
HVFET-ISOC VP @ Ids=2%Idss	Volts	5	0	0	0	1	6	-3.0	-2.3	-1.3	-1.0	-1.8	-1.6	-1.7	66.5m	
HVFET-ISOC BVgx @ Ig=10uA	Volts	5	0	0	0	1	6	-15.0	-15.0	-6.0	-1.0	-13.9	-13.5	-13.7	223.5m	
HVFET-ISOC n Ideality Factor		5	0	0	1	0	6	1.0	1.0	2.0	2.0	1.1	1.1	1.1	11.4m	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4PGB206068 STATION : 1
OPERATOR : 78395
TEMP : AMBIENT

LOG FILE : OWR4PGB206068
PAR FILE : [APTPRG.PAR]OWRPGB.PAR
LIM FILE : [APTPRG.LIM]OWRFET
COMMENTS : MESFET @POST GATE BOTTOM
OWR TEG-.5U MES. FET TEST @ POST GATE(R2 FIELDS)

DATE : 10-AUG-92
LOG DATE : 10-AUG-92
LOG TIME : 15:53:48
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION	UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOLIM	LOSPEC	HISPEC	HILIM	MIN	MAX	MEAN	STD DEV	COEF
HVFET-ISOC Idss @ V=3 Volts	mA/mm	6	0	0	0	0	6	170.0	170.0	290.0	290.0	223.8	261.4	240.2	14.8	
HVFET-ISOC GM0 @ Vgs=0	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	149.1	155.9	153.1	2.3	
HVFET-ISOC GM50 @Vgs=50%Idss	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	127.2	134.7	131.5	2.5	
HVFET-ISOC VP @ Ids=2%Idss	Volts	6	0	0	0	0	6	-3.0	-2.3	-1.3	-1.0	-2.2	-1.8	-2.0	143.0m	
HVFET-ISOC BVgx @ Ig=10uA	Volts	6	0	0	0	0	6	-15.0	-15.0	-6.0	-1.0	-13.9	-13.1	-13.4	307.3m	
HVFET-ISOC n Ideality Factor		0	0	0	0	0	0	1.0	1.0	2.0	2.0	2.0	1.0	0.0	0.0	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4PGB206067 STATION : 1
OPERATOR : 78395
TEMP : AMBIENT

LOG FILE : OWR4PGB206067
PAR FILE : [APTPRG.PAR]OWRPGB.PAR
LIM FILE : [APTPRG.LIM]OWRFET
COMMENTS : MESFET @POST GATE BOTTOM
OWR TEG-.5U MES. FET TEST @ POST GATE(R2 FIELDS)

DATE : 10-AUG-92
LOG DATE : 10-AUG-92
LOG TIME : 15:52:40
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION	UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOLIM	LOSPEC	HISPEC	HILIM	MIN	MAX	MEAN	STD DEV	COEF
HVFET-ISOC Idss @ V=3 Volts	mA/mm	6	0	0	0	0	6	170.0	170.0	290.0	290.0	182.8	223.2	203.6	15.7	
HVFET-ISOC GM0 @ Vgs=0	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	159.7	164.0	161.8	1.8	
HVFET-ISOC GM50 @Vgs=50%Idss	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	140.4	145.5	143.6	2.1	
HVFET-ISOC VP @ Ids=2%Idss	Volts	6	0	0	0	0	6	-3.0	-2.3	-1.3	-1.0	-1.8	-1.4	-1.6	132.9m	
HVFET-ISOC BVgx @ Ig=10uA	Volts	6	0	0	0	0	6	-15.0	-15.0	-6.0	-1.0	-13.5	-12.7	-13.2	333.3m	
HVFET-ISOC n Ideality Factor		0	0	0	0	0	0	1.0	1.0	2.0	2.0	2.0	1.0	0.0	0.0	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4PGB206066 STATION : 1
OPERATOR : 78395
TEMP : AMBIENT

LOG FILE : OWR4PGB206066
PAR FILE : [APTPRG.PAR]OWRPGB.PAR
LIM FILE : [APTPRG.LIM]OWRFET
COMMENTS : MESFET @POST GATE BOTTOM
OWR TEG-.5U MES. FET TEST @ POST GATE(R2 FIELDS)

DATE : 10-AUG-92
LOG DATE : 10-AUG-92
LOG TIME : 15:51:21
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION	UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOLIM	LOSPEC	HISPEC	HILIM	MIN	MAX	MEAN	STD DEV	COEF
HVFET-ISOC Idss @ V=3 Volts	mA/mm	6	0	0	0	0	6	170.0	170.0	290.0	290.0	198.7	226.0	208.2	10.8	
HVFET-ISOC GM0 @ Vgs=0	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	159.8	163.2	161.8	1.3	
HVFET-ISOC GM50 @Vgs=50%Idss	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	141.5	146.8	144.3	2.3	
HVFET-ISOC VP @ Ids=2%Idss	Volts	6	0	0	0	0	6	-3.0	-2.3	-1.3	-1.0	-1.8	-1.5	-1.6	97.0m	
HVFET-ISOC BVgx @ Ig=10uA	Volts	6	0	0	0	0	6	-15.0	-15.0	-6.0	-1.0	-13.5	-13.1	-13.3	223.6m	
HVFET-ISOC n Ideality Factor		0	0	0	0	0	0	1.0	1.0	2.0	2.0	2.0	1.0	0.0	0.0	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4PGB206064 STATION : 1
OPERATOR : 78395
TEMP : AMBIENT

LOG FILE : OWR4PGB206064
PAR FILE : [APTPRG.PAR]OWRPGB.PAR
LIM FILE : [APTPRG.LIM]OWRFET
COMMENTS : MESFET @POST GATE BOTTOM
OWR TEG-.5U MES. FET TEST @ POST GATE(R2 FIELDS)

DATE : 10-AUG-92
LOG DATE : 10-AUG-92
LOG TIME : 15:50:01
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION	UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOLIM	LOSPEC	HISPEC	HILIM	MIN	MAX	MEAN	STD DEV	COEF
HVFET-ISOC Idss @ V=3 Volts	mA/mm	5	0	0	1	0	6	170.0	170.0	290.0	290.0	175.1	248.5	212.1	31.9	1
HVFET-ISOC GM0 @ Vgs=0	mS/mm	4	2	0	0	0	6	90.0	120.0	300.0	300.0	95.3	168.6	142.1	35.1	2
HVFET-ISOC GM50 @Vgs=50%Idss	mS/mm	4	0	0	2	0	6	90.0	120.0	300.0	300.0	141.8	143.9	142.9	894.1m	
HVFET-ISOC VP @ Ids=2%Idss	Volts	3	0	1	2	0	6	-3.0	-2.3	-1.3	-1.0	-1.6	-1.1	-1.4	251.5m	1
HVFET-ISOC BVgx @ Ig=10uA	Volts	6	0	0	0	0	6	-15.0	-15.0	-6.0	-1.0	-14.7	-13.5	-14.0	421.6m	
HVFET-ISOC n Ideality Factor		0	0	0	0	0	0	1.0	1.0	2.0	2.0	2.0	1.0	0.0	0.0	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4PGB206063 STATION : 1
OPERATOR : 78395
TEMP : AMBIENT

LOG FILE : OWR4PGB206063
PAR FILE : [APTPRG.PAR]OWRPGB.PAR
LIM FILE : [APTPRG.LIM]OWRFET
COMMENTS : MESFET @POST GATE BOTTOM
OWR TEG-.5U MES. FET TEST @ POST GATE(R2 FIELDS)

DATE : 10-AUG-92
LOG DATE : 10-AUG-92
LOG TIME : 15:48:38
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION	UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOLIM	LOSPEC	HISPEC	HILIM	MIN	MAX	MEAN	STD DEV	COEF
HVFET-ISOC Idss @ V=3 Volts	mA/mm	6	0	0	0	0	6	170.0	170.0	290.0	290.0	217.2	251.4	231.4	15.6	
HVFET-ISOC GM0 @ Vgs=0	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	157.5	161.8	160.2	1.8	
HVFET-ISOC GM50 @Vgs=50%Idss	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	143.8	149.1	146.7	2.5	
HVFET-ISOC VP @ Ids=2%Idss	Volts	6	0	0	0	0	6	-3.0	-2.3	-1.3	-1.0	-2.0	-1.6	-1.8	140.0m	
HVFET-ISOC BVgx @ Ig=10uA	Volts	6	0	0	0	0	6	-15.0	-15.0	-6.0	-1.0	-13.9	-13.1	-13.6	333.2m	
HVFET-ISOC n Ideality Factor		0	0	0	0	0	0	1.0	1.0	2.0	2.0	2.0	1.0	0.0	0.0	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4PGB206062 STATION : 1
OPERATOR : 78395
TEMP : AMBIENT

LOG FILE : OWR4PGB206062
PAR FILE : [APTPRG.PAR]OWRPGB.PAR
LIM FILE : [APTPRG.LIM]OWRFET
COMMENTS : MESFET @POST GATE BOTTOM
OWR TEG-.5U MES. FET TEST @ POST GATE(R2 FIELDS)

DATE : 10-AUG-92
LOG DATE : 10-AUG-92
LOG TIME : 15:44:42
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION	UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOLIM	LOSPEC	HISPEC	HILIM	MIN	MAX	MEAN	STD DEV	COEF
HVFET-ISOC Idss @ V=3 Volts	mA/mm	6	0	0	0	0	6	170.0	170.0	290.0	290.0	190.8	230.5	212.1	14.4	
HVFET-ISOC GM0 @ Vgs=0	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	165.8	170.0	168.0	1.4	
HVFET-ISOC GM50 @Vgs=50%Idss	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	147.3	152.7	150.1	2.0	
HVFET-ISOC VP @ Ids=2%Idss	Volts	6	0	0	0	0	6	-3.0	-2.3	-1.3	-1.0	-1.7	-1.4	-1.6	114.4m	
HVFET-ISOC BVgx @ Ig=10uA	Volts	6	0	0	0	0	6	-15.0	-15.0	-6.0	-1.0	-13.9	-13.1	-13.5	307.3m	
HVFET-ISOC n Ideality Factor		0	0	0	0	0	0	1.0	1.0	2.0	2.0	2.0	1.0	0.0	0.0	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4FNT206068 STATION : 1
OPERATOR : 78395
TEMP : AMBIENT

LOG FILE : OWR4FNT206068
PAR FILE : [APTPRG.PAR]OWRFNT.PAR
LIM FILE : [APTPRG.LIM]OWRFET
COMMENTS : .5U MESFET @ FIRST NITRI
OWR TEG-.5U MES. FET TEST@1ST NITRIDE(R1 FIELDS)

DATE : 17-AUG-92
LOG DATE : 14-AUG-92
LOG TIME : 16:27:49
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION	UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOLIM	LOSPEC	HISPEC	HILIM	MIN	MAX	MEAN	STD DEV	COEF
HVFET-ISOC Idss @ V=3 Volts	mA/mm	6	0	0	0	0	6	170.0	170.0	290.0	290.0	232.6	287.2	263.5	19.0	
HVFET-ISOC GM0 @ Vgs=0	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	149.5	157.6	154.2	2.7	
HVFET-ISOC GM50 @Vgs=50%Idss	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	126.5	136.0	131.4	3.1	
HVFET-ISOC VP @ Ids=2%Idss	Volts	5	1	0	0	0	6	-3.0	-2.3	-1.3	-1.0	-2.4	-1.9	-2.1	184.0m	
HVFET-ISOC BVgx @ Ig=10uA	Volts	6	0	0	0	0	6	-15.0	-15.0	-6.0	-1.0	-13.5	-12.2	-12.9	428.1m	
HVFET-ISOC n Ideality Factor		6	0	0	0	0	6	1.0	1.0	2.0	2.0	1.2	1.2	1.2	14.8m	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4FNT206067 STATION : 1
OPERATOR : 78395
TEMP : AMBIENT

LOG FILE : OWR4FNT206067
PAR FILE : [APTPRG.PAR]OWRFNT.PAR
LIM FILE : [APTPRG.LIM]OWRFET
COMMENTS : .5U MESFET @ FIRST NITRI
OWR TEG-.5U MES. FET TEST@1ST NITRIDE(R1 FIELDS)

DATE : 17-AUG-92
LOG DATE : 14-AUG-92
LOG TIME : 16:26:30
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION	UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOLIM	LOSPEC	HISPEC	HILIM	MIN	MAX	MEAN	STD DEV	COEF
HVFET-ISOC Idss @ V=3 Volts	mA/mm	6	0	0	0	0	6	170.0	170.0	290.0	290.0	216.5	248.6	230.8	13.8	
HVFET-ISOC GM0 @ Vgs=0	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	157.5	165.6	161.7	3.6	
HVFET-ISOC GM50 @Vgs=50%Idss	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	144.1	153.1	148.2	4.1	
HVFET-ISOC VP @ Ids=2%Idss	Volts	6	0	0	0	0	6	-3.0	-2.3	-1.3	-1.0	-1.9	-1.6	-1.7	131.2m	
HVFET-ISOC BVgx @ Ig=10uA	Volts	6	0	0	0	0	6	-15.0	-15.0	-6.0	-1.0	-12.7	-11.8	-12.4	341.5m	
HVFET-ISOC n Ideality Factor		6	0	0	0	0	6	1.0	1.0	2.0	2.0	1.2	1.2	1.2	6.5m	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4FNT206066 STATION : 1
OPERATOR : 78395
TEMP : AMBIENT

LOG FILE : OWR4FNT206066
PAR FILE : [APTPRG.PAR]OWRFNT.PAR
LIM FILE : [APTPRG.LIM]OWRFET
COMMENTS : .5U MESFET @ FIRST NITRI
OWR TEG-.5U MES. FET TEST@1ST NITRIDE(R1 FIELDS)

DATE : 17-AUG-92
LOG DATE : 14-AUG-92
LOG TIME : 16:25:04
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION	UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOLIM	LOSPEC	HISPEC	HILIM	MIN	MAX	MEAN	STD DEV	COEF
HVFET-ISOC Idss @ V=3 Volts	mA/mm	6	0	0	0	0	6	170.0	170.0	290.0	290.0	209.7	253.5	232.3	14.3	
HVFET-ISOC GM0 @ Vgs=0	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	157.1	163.7	161.1	2.7	
HVFET-ISOC GM50 @Vgs=50%Idss	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	143.0	152.8	149.2	3.6	
HVFET-ISOC VP @ Ids=2%Idss	Volts	6	0	0	0	0	6	-3.0	-2.3	-1.3	-1.0	-1.9	-1.5	-1.7	128.9m	
HVFET-ISOC BVgx @ Ig=10uA	Volts	6	0	0	0	0	6	-15.0	-15.0	-6.0	-1.0	-13.5	-12.2	-12.9	428.1m	
HVFET-ISOC n Ideality Factor		6	0	0	0	0	6	1.0	1.0	2.0	2.0	1.2	1.2	1.2	8.5m	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4FNT206064 STATION : 1
OPERATOR : 78395
TEMP : AMBIENT

LOG FILE : OWR4FNT206064
PAR FILE : [APTPRG.PAR]OWRFNT.PAR
LIM FILE : [APTPRG.LIM]OWRFET
COMMENTS : .5U MESFET @ FIRST NITRI
OWR TEG-.5U MES. FET TEST@1ST NITRIDE(R1 FIELDS)

DATE : 17-AUG-92
LOG DATE : 14-AUG-92
LOG TIME : 16:23:43
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION	UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOLIM	LOSPEC	HISPEC	HILIM	MIN	MAX	MEAN	STD DEV	COEF
HVFET-ISOC Idss @ V=3 Volts	mA/mm	6	0	0	0	0	6	170.0	170.0	290.0	290.0	202.5	256.0	226.6	18.5	
HVFET-ISOC GM0 @ Vgs=0	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	156.2	165.2	160.8	3.5	
HVFET-ISOC GM50 @Vgs=50%Idss	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	140.8	147.3	144.4	2.4	
HVFET-ISOC VP @ Ids=2%Idss	Volts	6	0	0	0	0	6	-3.0	-2.3	-1.3	-1.0	-2.0	-1.5	-1.7	155.7m	
HVFET-ISOC BVgx @ Ig=10uA	Volts	6	0	0	0	0	6	-15.0	-15.0	-6.0	-1.0	-13.5	-12.7	-13.1	307.2m	
HVFET-ISOC n Ideality Factor		6	0	0	0	0	6	1.0	1.0	2.0	2.0	1.2	1.2	1.2	13.6m	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4FNT206063 STATION : 1
OPERATOR : 78395
TEMP : AMBIENT

LOG FILE : OWR4FNT206063
PAR FILE : [APTPRG.PAR]OWRFNT.PAR
LIM FILE : [APTPRG.LIM]OWRFET
COMMENTS : .5U MESFET @ FIRST NITRI
OWR TEG-.5U MES. FET TEST@1ST NITRIDE(R1 FIELDS)

DATE : 17-AUG-92
LOG DATE : 14-AUG-92
LOG TIME : 16:22:21
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION	UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOLIM	LOSPEC	HISPEC	HILIM	MIN	MAX	MEAN	STD DEV	COEF
HVFET-ISOC Idss @ V=3 Volts	mA/mm	6	0	0	0	0	6	170.0	170.0	290.0	290.0	231.1	275.9	255.8	16.9	
HVFET-ISOC GM0 @ Vgs=0	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	152.3	164.1	158.2	4.9	
HVFET-ISOC GM50 @Vgs=50%Idss	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	142.2	156.2	149.2	6.1	
HVFET-ISOC VP @ Ids=2%Idss	Volts	6	0	0	0	0	6	-3.0	-2.3	-1.3	-1.0	-2.1	-1.7	-1.9	172.8m	
HVFET-ISOC BVgx @ Ig=10uA	Volts	6	0	0	0	0	6	-15.0	-15.0	-6.0	-1.0	-12.7	-11.4	-12.0	428.1m	
HVFET-ISOC n Ideality Factor		6	0	0	0	0	6	1.0	1.0	2.0	2.0	1.2	1.2	1.2	6.4m	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4FNT206062 STATION : 1
OPERATOR : 78395
TEMP : AMBIENT

LOG FILE : OWR4FNT206062
PAR FILE : [APTPRG.PAR]OWRFNT.PAR
LIM FILE : [APTPRG.LIM]OWRFET
COMMENTS : .5U MESFET @ FIRST NITRI
OWR TEG-.5U MES. FET TEST@1ST NITRIDE(R1 FIELDS)

DATE : 17-AUG-92
LOG DATE : 14-AUG-92
LOG TIME : 16:20:16
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION	UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOLIM	LOSPEC	HISPEC	HILIM	MIN	MAX	MEAN	STD DEV	COEF
HVFET-ISOC Idss @ V=3 Volts	mA/mm	5	0	0	0	.1	6	170.0	170.0	290.0	290.0	232.9	248.9	240.6	7.5	
HVFET-ISOC GM0 @ Vgs=0	mS/mm	5	0	0	0	1	6	90.0	120.0	300.0	300.0	159.7	165.8	162.9	2.5	
HVFET-ISOC GM50 @Vgs=50%Idss	mS/mm	5	0	0	0	1	6	90.0	120.0	300.0	300.0	145.6	151.5	149.1	2.3	
HVFET-ISOC VP @ Ids=2%Idss	Volts	5	0	0	0	1	6	-3.0	-2.3	-1.3	-1.0	-1.9	-1.7	-1.8	68.4m	
HVFET-ISOC BVgx @ Ig=10uA	Volts	5	0	0	0	1	6	-15.0	-15.0	-6.0	-1.0	-12.7	-12.2	-12.3	182.5m	
HVFET-ISOC n Ideality Factor		5	0	0	1	0	6	1.0	1.0	2.0	2.0	1.1	1.2	1.2	13.4m	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4FNB206068 STATION : 1
OPERATOR : 78395
TEMP : AMBIENT

LOG FILE : OWR4FNB206068
PAR FILE : [APTPRG.PAR]OWRFNB.PAR
LIM FILE : [APTPRG.LIM]OWRFET
COMMENTS : .5U MESFET @ FIRST NITRI
OWR TEG-.5U MES. FET TEST@1ST NITRIDE(R2 FIELDS)

DATE : 17-AUG-92
LOG DATE : 14-AUG-92
LOG TIME : 16:50:13
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION	UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOLIM	LOSPEC	HISPEC	HILIM	MIN	MAX	MEAN	STD DEV	COEF
HVFET-ISOC Idss @ V=3 Volts	mA/mm	6	0	0	0	0	6	170.0	170.0	290.0	290.0	243.7	279.4	259.4	14.2	
HVFET-ISOC GM0 @ Vgs=0	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	152.8	161.4	157.3	2.8	
HVFET-ISOC GM50 @Vgs=50%Idss	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	130.2	137.5	134.7	2.6	
HVFET-ISOC VP @ Ids=2%Idss	Volts	6	0	0	0	0	6	-3.0	-2.3	-1.3	-1.0	-2.3	-1.9	-2.1	141.5m	
HVFET-ISOC BVgx @ Ig=10uA	Volts	6	0	0	0	0	6	-15.0	-15.0	-6.0	-1.0	-13.1	-12.2	-12.7	365.0m	
HVFET-ISOC n Ideality Factor		0	0	0	0	0	0	1.0	1.0	2.0	2.0	2.0	1.0	0.0	0.0	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4FNB206067 STATION : 1
OPERATOR : 78395
TEMP : AMBIENT

LOG FILE : OWR4FNB206067
PAR FILE : [APTPRG.PAR]OWRFNB.PAR
LIM FILE : [APTPRG.LIM]OWRFET
COMMENTS : .5U MESFET @ FIRST NITRI
OWR TEG-.5U MES. FET TEST@1ST NITRIDE(R2 FIELDS)

DATE : 17-AUG-92
LOG DATE : 14-AUG-92
LOG TIME : 16:49:07
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION	UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOLIM	LOSPEC	HISPEC	HILIM	MIN	MAX	MEAN	STD DEV	COEF
HVFET-ISOC Idss @ V=3 Volts	mA/mm	6	0	0	0	0	6	170.0	170.0	290.0	290.0	204.2	243.5	224.2	15.4	
HVFET-ISOC GM0 @ Vgs=0	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	160.9	167.0	163.8	2.5	
HVFET-ISOC GM50 @Vgs=50%Idss	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	145.4	151.2	149.1	2.4	
HVFET-ISOC VP @ Ids=2%Idss	Volts	6	0	0	0	0	6	-3.0	-2.3	-1.3	-1.0	-1.8	-1.5	-1.7	130.3m	
HVFET-ISOC BVgx @ Ig=10uA	Volts	6	0	0	0	0	6	-15.0	-15.0	-6.0	-1.0	-13.1	-11.8	-12.4	494.3m	
HVFET-ISOC n Ideality Factor		0	0	0	0	0	0	1.0	1.0	2.0	2.0	2.0	1.0	0.0	0.0	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4FNB206066 STATION : 1
OPERATOR : 78395
TEMP : AMBIENT

LOG FILE : OWR4FNB206066
PAR FILE : [APTPRG.PAR]OWRFNB.PAR
LIM FILE : [APTPRG.LIM]OWRFET
COMMENTS : .5U MESFET @ FIRST NITRI
OWR TEG-.5U MES. FET TEST@1ST NITRIDE(R2 FIELDS)

DATE : 17-AUG-92
LOG DATE : 14-AUG-92
LOG TIME : 16:47:50
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION	UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOLIM	LOSPEC	HISPEC	HILIM	MIN	MAX	MEAN	STD DEV	COEF
HVFET-ISOC Idss @ V=3 Volts	mA/mm	6	0	0	0	0	6	170.0	170.0	290.0	290.0	220.8	246.7	229.3	10.6	
HVFET-ISOC GM0 @ Vgs=0	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	161.3	166.1	163.1	1.8	
HVFET-ISOC GM50 @Vgs=50%Idss	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	146.4	151.7	149.4	2.4	
HVFET-ISOC VP @ Ids=2%Idss	Volts	6	0	0	0	0	6	-3.0	-2.3	-1.3	-1.0	-1.9	-1.6	-1.7	100.1m	
HVFET-ISOC BVgx @ Ig=10uA	Volts	6	0	0	0	0	6	-15.0	-15.0	-6.0	-1.0	-13.1	-12.2	-12.6	307.3m	
HVFET-ISOC n Ideality Factor		0	0	0	0	0	0	1.0	1.0	2.0	2.0	2.0	1.0	0.0	0.0	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4FNB206064 STATION : 1
OPERATOR : 78395
TEMP : AMBIENT

LOG FILE : OWR4FNB206064
PAR FILE : [APTPRG.PAR]OWRFNB.PAR
LIM FILE : [APTPRG.LIM]OWRFET
COMMENTS : .5U MESFET @ FIRST NITRI
OWR TEG-.5U MES. FET TEST@1ST NITRIDE(R2 FIELDS)

DATE : 17-AUG-92
LOG DATE : 14-AUG-92
LOG TIME : 16:46:29
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION	UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOLIM	LOSPEC	HISPEC	HILIM	MIN	MAX	MEAN	STD DEV	COEF
HVFET-ISOC Idss @ V=3 Volts	mA/mm	5	0	0	1	0	6	170.0	170.0	290.0	290.0	194.3	258.2	227.5	27.1	1
HVFET-ISOC GM0 @ Vgs=0	mS/mm	4	2	0	0	0	6	90.0	120.0	300.0	300.0	90.9	171.1	141.6	38.2	2
HVFET-ISOC GM50 @Vgs=50%Idss	mS/mm	4	0	0	2	0	6	90.0	120.0	300.0	300.0	145.6	149.8	148.0	1.9	
HVFET-ISOC VP @ Ids=2%Idss	Volts	3	0	1	2	0	6	-3.0	-2.3	-1.3	-1.0	-1.7	-1.1	-1.5	246.9m	1
HVFET-ISOC BVgx @ Ig=10uA	Volts	6	0	0	0	0	6	-15.0	-15.0	-6.0	-1.0	-14.3	-12.7	-13.4	542.5m	
HVFET-ISOC n Ideality Factor		0	0	0	0	0	0	1.0	1.0	2.0	2.0	2.0	1.0	0.0	0.0	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4FNB206063 STATION : 1
OPERATOR : 78395
TEMP : AMBIENT

LOG FILE : OWR4FNB206063
PAR FILE : [APTPRG.PAR]OWRFNB.PAR
LIM FILE : [APTPRG.LIM]OWRFET
COMMENTS : .5U MESFET @ FIRST NITRI
OWR TEG-.5U MES. FET TEST@1ST NITRIDE(R2 FIELDS)

DATE : 17-AUG-92
LOG DATE : 14-AUG-92
LOG TIME : 16:45:12
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION	UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOLIM	LOSPEC	HISPEC	HILIM	MIN	MAX	MEAN	STD DEV	COEF
HVFET-ISOC Idss @ V=3 Volts	mA/mm	6	0	0	0	0	6	170.0	170.0	290.0	290.0	236.0	269.0	249.7	15.3	
HVFET-ISOC GM0 @ Vgs=0	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	156.6	162.2	159.9	2.5	
HVFET-ISOC GM50 @Vgs=50%Idss	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	146.6	152.5	149.8	2.7	
HVFET-ISOC VP @ Ids=2%Idss	Volts	6	0	0	0	0	6	-3.0	-2.3	-1.3	-1.0	-2.0	-1.7	-1.9	136.1m	
HVFET-ISOC BVgx @ Ig=10uA	Volts	6	0	0	0	0	6	-15.0	-15.0	-6.0	-1.0	-12.7	-11.4	-12.0	428.1m	
HVFET-ISOC n Ideality Factor		0	0	0	0	0	0	1.0	1.0	2.0	2.0	2.0	1.0	0.0	0.0	

TRW ADVANCED MICROELECTRONICS LABORATORY
LOT ID : OWR-4
WAFER : OWR4FNB206062 STATION : 1
OPERATOR : 78395
TEMP : AMBIENT

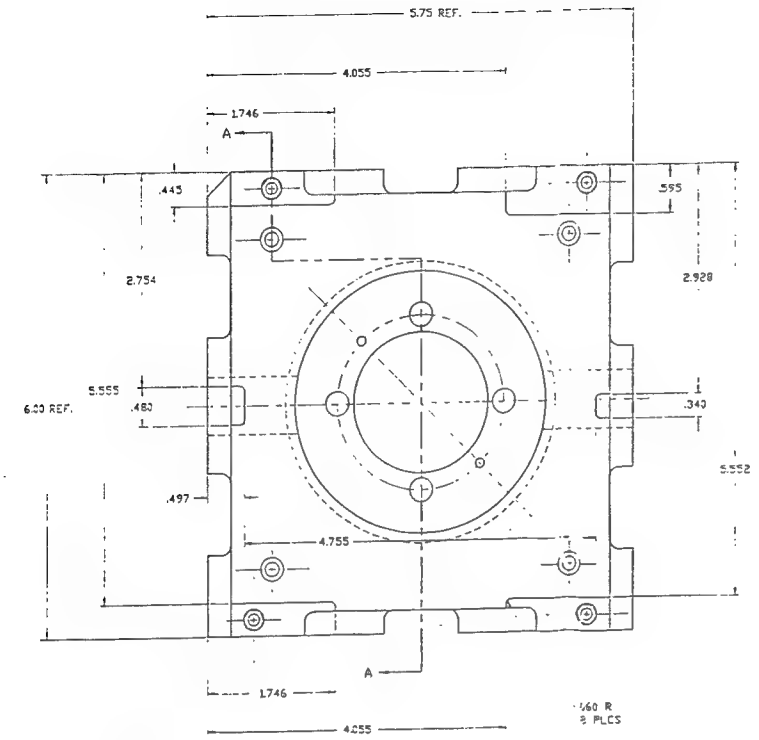
LOG FILE : OWR4FNB206062
PAR FILE : [APTPRG.PAR]OWRFNB.PAR
LIM FILE : [APTPRG.LIM]OWRFET
COMMENTS : .5U MESFET @ FIRST NITRI
OWR TEG-.5U MES. FET TEST@1ST NITRIDE(R2 FIELDS)

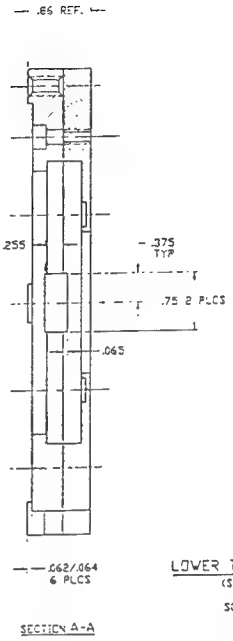
DATE : 17-AUG-92
LOG DATE : 14-AUG-92
LOG TIME : 16:43:47
WAFLAT : BOTTOM
PAGE : 1

DEVICE DESCRIPTION	UNITS	PASS	LOW	HIGH	NFTN	TERR	TOTL	LOLIM	LOSPEC	HISPEC	HILIM	MIN	MAX	MEAN	STD DEV	COEF
HVFET-ISOC Idss @ V=3 Volts	mA/mm	6	0	0	0	0	6	170.0	170.0	290.0	290.0	211.9	249.4	232.5	13.9	
HVFET-ISOC GM0 @ Vgs=0	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	164.0	169.3	166.4	2.0	
HVFET-ISOC GM50 @Vgs=50%Idss	mS/mm	6	0	0	0	0	6	90.0	120.0	300.0	300.0	147.8	154.7	151.2	2.6	
HVFET-ISOC VP @ Ids=2%Idss	Volts	6	0	0	0	0	6	-3.0	-2.3	-1.3	-1.0	-1.8	-1.6	-1.7	110.8m	
HVFET-ISOC BVgx @ Ig=10uA	Volts	6	0	0	0	0	6	-15.0	-15.0	-6.0	-1.0	-13.1	-11.8	-12.5	494.3m	
HVFET-ISOC n Ideality Factor		0	0	0	0	0	0	1.0	1.0	2.0	2.0	2.0	1.0	0.0	0.0	

APPENDIX B

Drawings for On-Wafer Lifetest Fixture





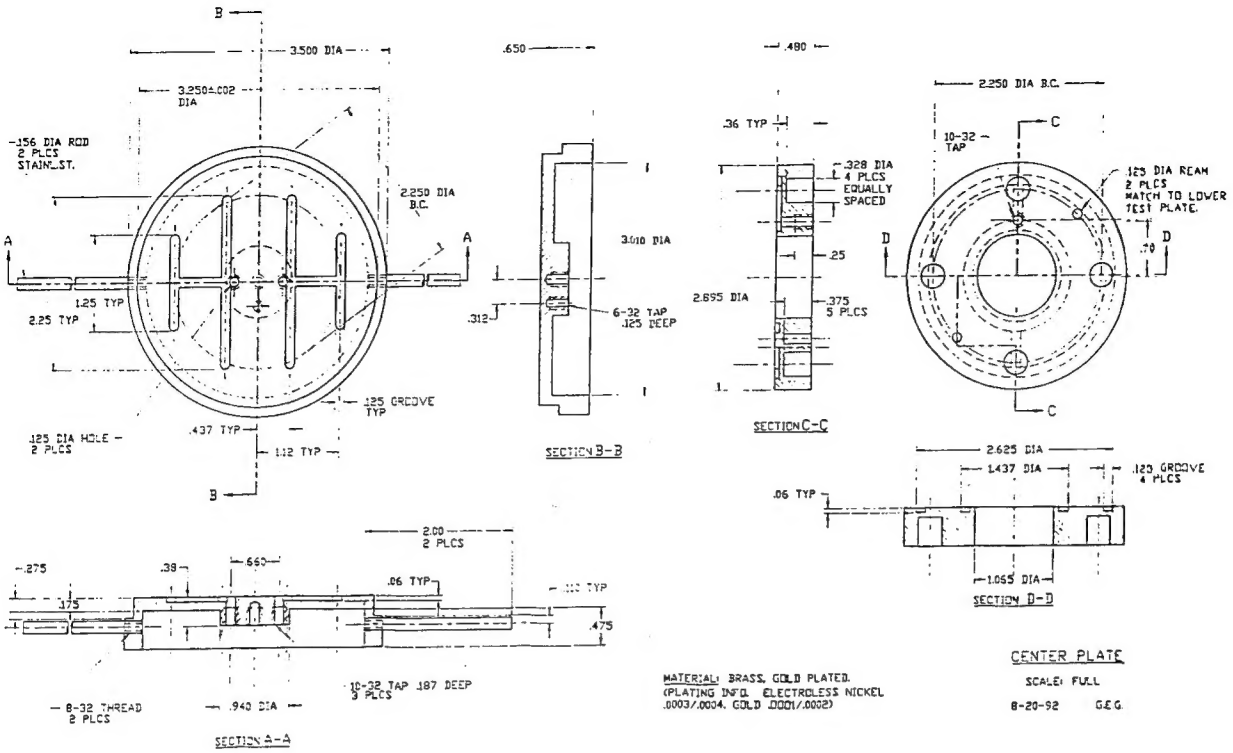
SECTION A-A

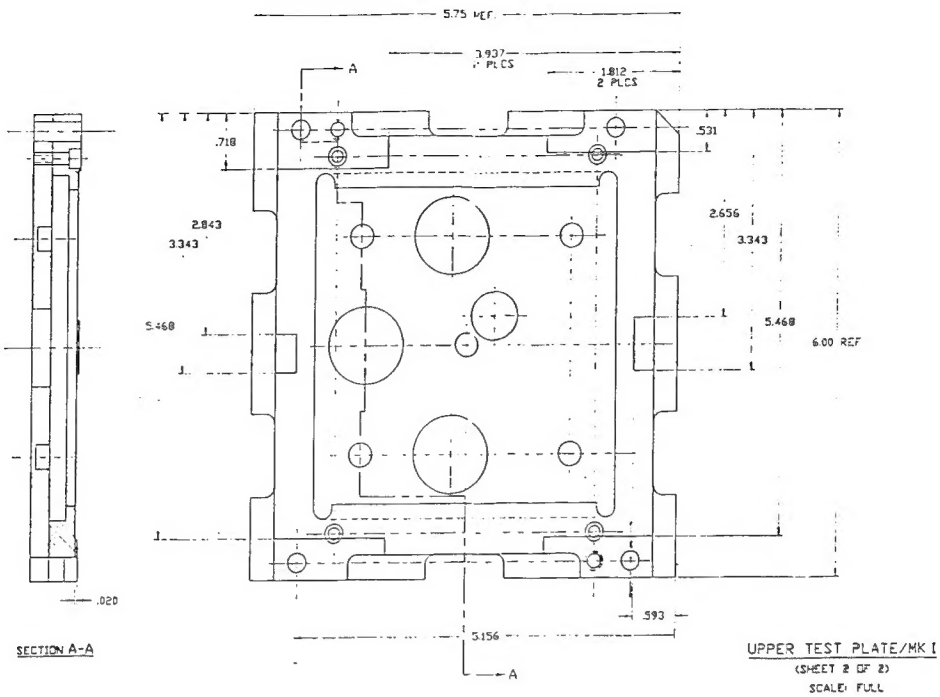
MATERIAL: STAINLESS STEEL

LOWER TEST PLATE/MK I
(SHEET 2 OF 2)

SCALE FULL

8-24-92 GI G


B
3.500 DIA
3.250+.002
DIA
.156 DIA ROD
2 PLCS
STAINLST.
2.250 DIA
B.C.
A
A
1.25 TYP
2.25 TYP
.125 GROOVE
TYP
.125 DIA HOLE
2 PLCS
.437 TYP
1.12 TYP
B
.650
3.010 DIA
.312
6-32 TAP
.125 DEEP
SECTION B-B
.490
.36 TYP
.328 DIA
4 PLCS
EQUALLY
SPACED
.25
2.895 DIA
.375
5 PLCS
SECTION C-C
2.250 DIA B.C.
10-32
TAP
C
C
.125 DIA REAM
2 PLCS
MATCH TO LOWER
TEST PLATE.
.20
D
D
2.625 DIA
1.437 DIA
.120 GROOVE
4 PLCS
.06 TYP
1.055 DIA
SECTION D-D
2.00
2 PLCS
.275
.38
.660
.06 TYP
.375
.475
10-32 TAP .187 DEEP
3 PLCS
8-32 THREAD
2 PLCS
.940 DIA
SECTION A-A
MATERIAL: BRASS, GOLD PLATED.
(PLATING INFO. ELECTROLESS NICKEL
.0003/.0004, GOLD .0001/.0002)
CENTER PLATE
SCALE: FULL
8-20-92
G.E.G.


5.75 REF.
3.937
2 PLCS
1.812
2 PLCS
A
.718
.531
2.843
3.343
2.656
3.343
5.468
5.468
6.00 REF
.020
.593
3.156
A
SECTION A-A
UPPER TEST PLATE/MK I
(SHEET 2 OF 2)
SCALE: FULL
8-11-98
G.E.G.

Rome Laboratory

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Organization POC: _____(Optional)

Address:_____

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Rating_____

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If yes, please identify the area(s), and comment on what aspects make them "stand out."

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